

**CONTROLLED
DOCUMENT**

TI 6490.41

INSTRUCTION BOOK

MAINTENANCE AND DIAGNOSTIC TEST SET

PART OF

**MODEL 1 FULL CAPACITY FLIGHT SERVICE
AUTOMATION SYSTEM**

CONTRACT DTFA01-81-C 10039

CONTRACTOR

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MADE FOR

**U.S. DEPARTMENT OF TRANSPORTATION
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26-1	MUX Diagnostic Error Message Description.	26-8
26-2	Test Connector Substituting Table	26-16
31-1	Initial Switch Settings	31-2

SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION. This manual provides operating and maintenance instructions for the Maintenance and Diagnostic Test Set (MADTS), for the Model 1 Full Capacity (M1FC) Flight Service Automated System (FSAS). The manual includes instruction for the off-line testing and troubleshooting of LRU's that have been removed from the FSAS, after being identified as failed by the system diagnostic software.

1.2 DESCRIPTION. The MADTS is a self-contained test set in a standard single-bay rack, requiring only an electrical power input to perform test functions. The unit may be located near an area for testing larger LRU's or near a work bench for testing smaller LRU's. The MADTS has resident software which exercises the LRU under test in a simulated operational configuration. This allows the technician to determine the cause of failure and take appropriate repair measures. The MADTS performs a brief self-test on power-up to ensure proper operation during LRU testing.

The MADTS is shown in Figure 1-1 with major assemblies identified in Table 1-1.

1.2.1 Electrical Characteristics. Table 1-2 lists the electrical characteristics of the MADTS.

1.2.2 Physical Characteristics. Table 1-3 lists the physical characteristics of the MADTS.

1.3 EQUIPMENT SUPPLIED. Table 1-4 lists the equipment supplied as parts of the MADTS.

1.4 EQUIPMENT REQUIRED BUT NOT SUPPLIED. Table 1-5 is a list of equipment required for use with the MADTS which is not supplied.

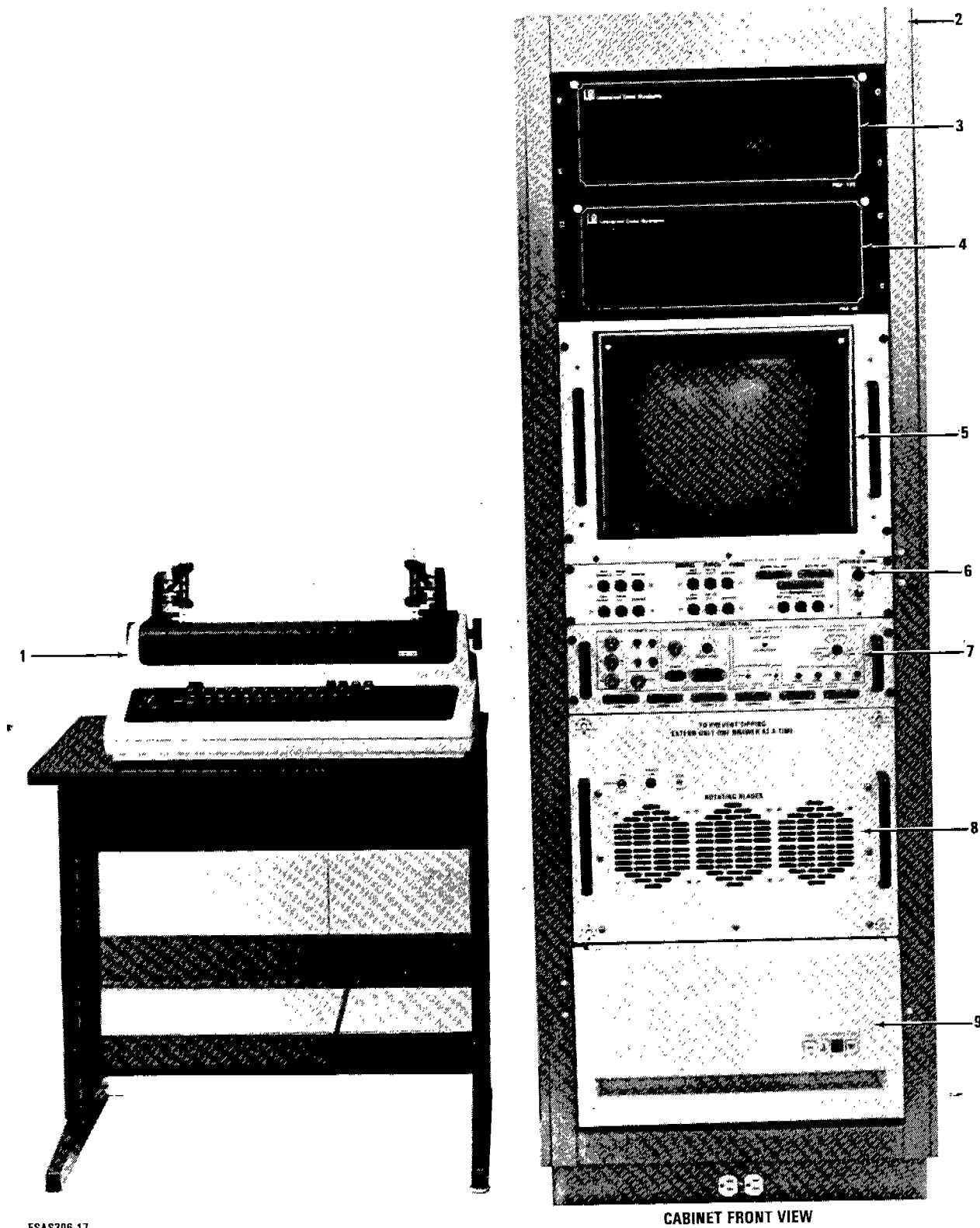
1.5 APPLICATION. The MADTS is capable of testing 24 LRU's in an on-line configuration. The resident diagnostic software exercises the LRU under test in a complete functional test to allow trained technical personnel to verify malfunctions. The LRU's which are testable on the MADTS are listed in Table 1-6.

CAUTION

While MADTS is capable of testing certain LRUs in an on-line configuration with resident diagnostic software, the following steps must be taken prior to testing any LRU.

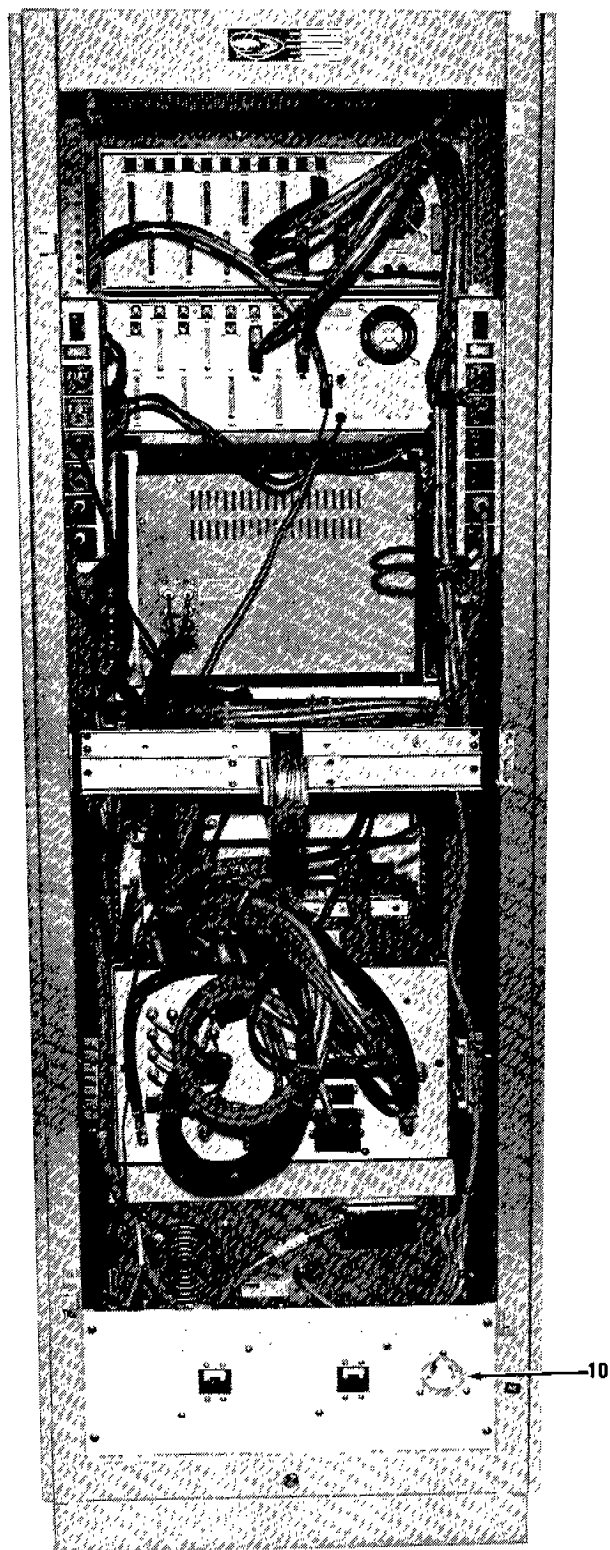
1. Read failure report which accompanied the failed LRU.
2. Inspect the LRU for physical damage.
3. Inspect the LRU for mechanical damage.
4. Inspect the LRU for electrical damage.

When obvious damage is noted, refer to the appropriate LRU technical instruction book (Refer to Table 1-1 in the M1FC FSAS System Book TI 6490.36) and take appropriate corrective action. Failure to do so may result in further damage to the LRU and, if connected to the MADTS, may damage the MADTS.



FSAS306-17

Figure 1-1. Maintenance and Diagnostic Test Set (MADTS)
(Sheet 1 of 2)



FSAS306-18

CABINET BACK VIEW

Figure 1-1. Maintenance and Diagnostic Test Set (MADTS)
(Sheet 2 of 2)

Table 1-1

Maintenance and Diagnostic Test Set (MADTS)
Major Assemblies

Fig. 1-1 Reference	Reference Designator	Part/Model Number	Nomenclature
1	N/A	LA34-AA/ LA100-CA	Printer Terminal
2	N/A	401-37571-01	MADTS Rack Assembly
3	1A7	RM-12E	Modem Enclosure
4	1A6	RM-8E	Modem Enclosure
5	1A5	401-37566-01	Monitor Assembly
6	1A4	401-37844-01	Digital Patch Panel Assembly
7	1A3	401-37575-01	I/O Control Panel Assembly
8	1A2	401-36720-01	Electronics Chassis
9	1A1	RL01-AK/ RL02-AK	Disk Drive
10	1A8	401-37757-01	AC J-Box

Table 1-2

MADTS Electrical Characteristics

Power Requirements:	110 Vac @20 amperes
DC Output Voltages:	+5 Vdc, <u>+12</u> Vdc
Modem Loop Output (dBm):	1, -2, -4, -6, -8, -10, -12.

Table 1-3

MADTS Physical Characteristics

Height:	69.875 in.
Width:	22.25 in.
Depth:	37 1/4 in.
Weight:	500 lbs.
Operating Temperature Limits:	+15°C. to +32°C.

Table 1-4. MADTS Equipment Supplied

Nomenclature	Reference Designator	Part/Model Number	Qty.	Manufacturer
MADTS Rack Assembly	UNIT 1	401-37571-01	1	E-Systems
Disk Drive	1A1	RL01-AK/RL02-AK	1	Digital Equipment
Multiplexer Printed Circuit Board (PCB)	1A2A1A2UL2	401-36993-03	1	E-Systems
Alphanumeric On-The-Fly (A/N OTF) Processor PCB	1A2A1A3UL3	401-33676-01	1	E-Systems
Quad Cache PCB	1A2A1A4UL1	401-33692-01	1	E-Systems
64K Word RAM Memory/Parity PCB	1A2A1A1L2	MSV11-LF	1	Digital Equipment
LSI-11/23 Processor (CPU) PCB	1A2A1A1L1	KDF11-AA	1	Digital Equipment
8-Channel Serial I/O PCB	1A2A1A1L3	8S	1	Technical Magic
DMA Controller Module PCB	1A2A1A1U3 1A2A1A1U4	DMA-QB	2	Peritek
Disk Controller PCB	1A2A1A2UL1	RLV12	1	Digital Equipment
32K Word PROM Memory PCB	1A2A1A3U4	MRV11-C	1	Digital Equipment
Power Fail-Restart Module PCB	1A2A1A3L4	KPV11-B	1	Digital Equipment
High Density Parallel Interface PCB	1A2A1A1L4	DRV11-J	1	Digital Equipment
Inter-Processor Buffer	1A2A1A1U2	IPB-11	1	Peritek
DMA 6-Channel Adapter	1A2A1A1U1	HEX-L11	1	Peritek
Bus Grant Board CCA	1A2A1A2L3	401-37909-09	1	E-Systems

Table 1-4. MADTS Equipment Supplied (Continued)

Nomenclature	Reference Designator	Part/Model Number	Qty.	Manufacturer
Bus Grant Board PWB	1A2A1A2U3 1A2A1A2U4 1A2A1A2L4	401-37909-09	3	E-Systems
Cable Assembly, DMA Interface	1A2W11 1A2W12	401-37767-01	2	E-Systems
Ribbon Cable Assembly	1A2W13 1A2W16	401-37762-01	4	E-Systems
Cable Assembly, Mux Interface	1A2W9 1A2W10	401-37759-01	2	E-Systems
Cable Assy, Unit Select	1A2W24	401-37782-01	1	E-Systems
RM-208A Modem		2082278	1	Universal Data Systems
RM-A/O Auto Call/Auto Ans. Unit		1020364	1	Universal Data Systems
RM-800 Manual Call Up Unit		1020377	1	Universal Data Systems
Disk Controller		SC01-B1	1	EMULEX
Tape Controller		TC01	1	EMULEX
Cable Assy, Test, CTS, Clock No. 2		401-37876-01	1	E-Systems
Cable Assy, Serial I/O (LA-34)		401-37126-19	1	E-Systems
I/O Cable, Multiplexer		401-37142-02	2	E-Systems
Cable Assy, Power Mux		401-37739-01	1	E-Systems
Cable Assy, Test Kennedy Tape Drive, Control		401-37845	1	E-Systems
Cable Assy, Test MSD		DPC-32-M-6FT-M2	1	Dynatech

Table 1-4. MADTS Equipment Supplied (Continued)

Nomenclature	Reference Designator	Part/Model Number	Qty.	Manufacturer
Cable Assy, Test Kennedy Tape Drive, Data	UNIT 2	401-37846	1	E-Systems
Cable Assy, Test Ampex Disk Drive, Data		401-37847	1	E-Systems
Cable Assy, Test Ampex Disk Drive, Control		401-37848	1	E-Systems
Cable Assy, Test CTS, Clock # 1		401-37849	1	E-Systems
Cable Assy, Test Loop Back, 4 position		401-37863	2	E-Systems
Cable Assy, Test Loop Back, 3 position		401-37864	1	E-Systems
Cable Assy, Kennedy Tape Drive, Loopback		401-37872	1	E-Systems
Cable Assy, Test, Mux Interface		401-37881-01	1	E-Systems
Cable Assy, Test, Power, Keyboard		401-37865	1	E-Systems
Cable, Keyboard Interconnect		401-36738-01	1	E-Systems
Cable, Video		401-36797-02	5	E-Systems
32 Circuit Patch Cord		DPC-32-Y	1	
Extender Board (Full Slot)		W987-00	1	
Extender Board (Half Slot)		W984-00	2	
Input/Output Terminal		LA34-AA	1	Digital Equipment
Printer Stand		LA10X-SL	1	Digital Equipment
Printer Tractor Feed		LAX34-AL	1	Digital Equipment

Table 1-5

Test Equipment Required
But Not Supplied

<u>Equipment</u>	<u>Manufacturer and Model No.</u>
Oscilloscope	Tektronix 2235
Multimeter	Fluke 8021B
Logic Analyzer	Hewlett-Packard 1630G with a 10269A Preprocessor and option 055 (8085)

Table 1-6

MADTS Testable Equipment

<u>Equipment</u>	<u>Manufacturer</u>	<u>Model or Part Number</u>
A/N OTF Processor	E-Systems	401-33676
A/N Quad Cache	E-Systems	401-33692
Multiplexer	E-Systems	401-36993
Coded Time Source Interface	E-Systems	401-37207
Keyboard Unit	E-Systems	401-36735
8-Channel Serial I/O	Technical Magic	8S
Power Fail-Restart Module	Digital Equipment	KPV11-B
Line Printer	Printronix	P-300
Magnetic Tape Drive	Kennedy	9000
Magnetic Disk Drive	Ampex	DM 9300 TD
Printer Terminal	Digital Equipment	LA34-AA/LA100-CA
DMA Controller Module	Peritek	DMA-QB
Multiprocessor Linking System	Peritek	HEX-L11
32K Word PROM Memory	Digital Equipment	MRV11-C
64K Word RAM Memory/Parity	Digital Equipment	MSV11-LF
LSI-11/23 Processor (CPU)	Digital Equipment	KDF11-AA
Disk Controller	Digital Equipment	RLV12
Disk Drive	Digital Equipment	RL01-AK/RL02-AK
Multiplexer Interface	E-Systems	401-37170
RL01/RL02 Disk Cartridge	Digital Equipment	RL01/RL02 Cartridge
Modem Card	Universal Data Systems	RM-9600
Modem Card	Universal Data Systems	RM-208
Modem Card	Universal Data Systems	RM-A/O
Modem Card	Universal Data Systems	RM-800
Modem Card	Universal Data Systems	RM-9600E FP
Modem Sharing Device	Universal Data Systems	2005064
Monitor	Ball	TTL150

SECTION II

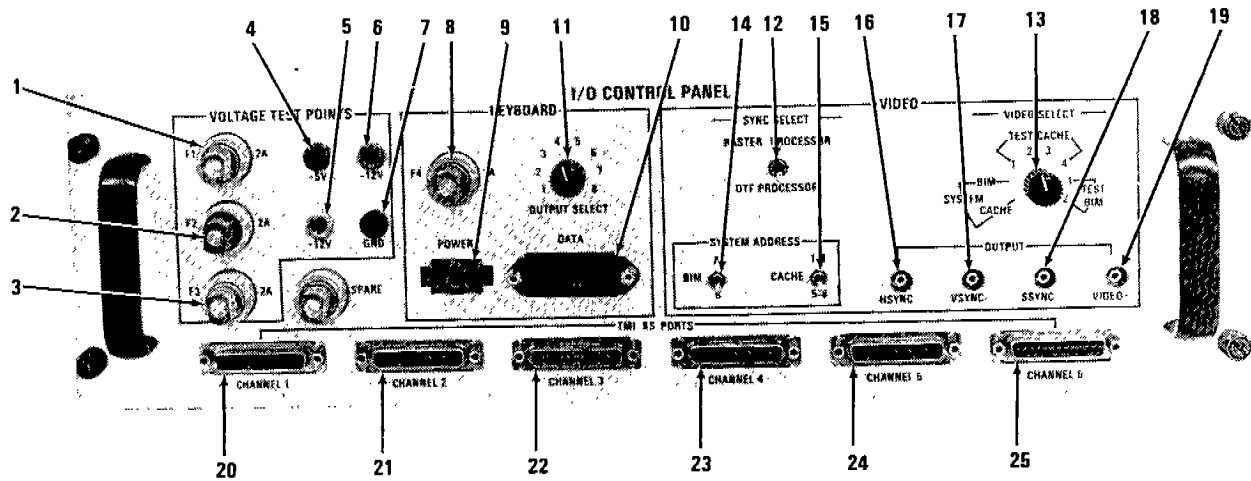
OPERATING INSTRUCTIONS

2.1 INTRODUCTION. The MADTS design allows ease of operation by maintenance personnel. A short introductory period enables the technician to operate the MADTS without special training. However, the software-controlled computer-type equipment requires strict adherence to procedures for proper operation.

2.2 CONTROLS AND INDICATORS. The controls, indicators, and PCB layout for the MADTS assemblies are shown in the figures and tables listed below.

<u>MADTS Assembly</u>	<u>Figure Number</u>	<u>Table Number</u>
I/O Control Panel	2-1	2-1
Electronics Chassis	2-2	2-2
Electronics Chassis PCB Layout	2-3	2-3
Digital Patch Panel	2-4	2-4
RL01/RL02 Disk Drive	2-5	2-5

2.3 OPERATING PROCEDURES. The power-up and self-test procedures for the MADTS are contained in Table 2-6. Procedures for test of individual LRUs are provided in the applicable manual section for the LRU under test.



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Figure 2-1. I/O Control Panel

Table 2-1
I/O Control Panel
Controls and Indicators

Fig. 2-1 Reference	Control or Indicator	Function
	VOLTAGE TEST POINTS	
1	F1	+5 VDC Fuse
2	F2	+12 VDC Fuse
3	F3	-12 VDC Fuse
4	+5V	+5 VDC Test Point
5	+12V	+12 VDC Test Point
6	-12V	-12 VDC Test Point
7	GND	Ground reference
	KEYBOARD	
8	F4	Keyboard Power Fuse
9	POWER	Keyboard Power Connector
10	DATA	Keyboard Data Connector
11	OUTPUT SELECT	Keyboard Output Select Switch
	VIDEO	
12	SYNC SELECT	Video Sync Source Select Switch
	RASTER PROCESSOR	Video Sync Supplied by MADTS Raster processor being tested
	OTF PROCESSOR	Video Sync supplied by MADTS OTF processor
13	VIDEO SELECT	Selects source of video to be supplied to Display
	SYSTEM CACHE	Video Source
	BIM	Video Source
	TEST CACHE 1-4	Video Source
	TEST BIM 1-2	Video Source
	SYSTEM ADDRESS	
14	BIM	BIM address select switch
	A	Position A selects BIM address 1, 2
	B	Position B selects BIM address 3, 4
15	CACHE	CACHE address select switch

Table 2-1 (Continued)

I/O Control Panel
Controls and Indicators

Fig. 2-1 Reference	Control or Indicator	Function
	1-4	Position 1-4 selects System CACHE address 1-4
	5-8	Position 5-8 selects System CACHE address 5-8
	OUTPUT	
16	HSYNC --	MADTS Horizontal Sync test output
17	VSYSN --	MADTS Vertical Sync test output
18	SSYSN --	MADTS System Sync test output
19	VIDEO+	System CACHE 2 Video test output
	TMI 8S PORTS	
20	CHANNEL 1	Full-Duplex Serial I/O Ports, channels 1 through 6
21	CHANNEL 2	
22	CHANNEL 3	
23	CHANNEL 4	
24	CHANNEL 5	
25	CHANNEL 6	

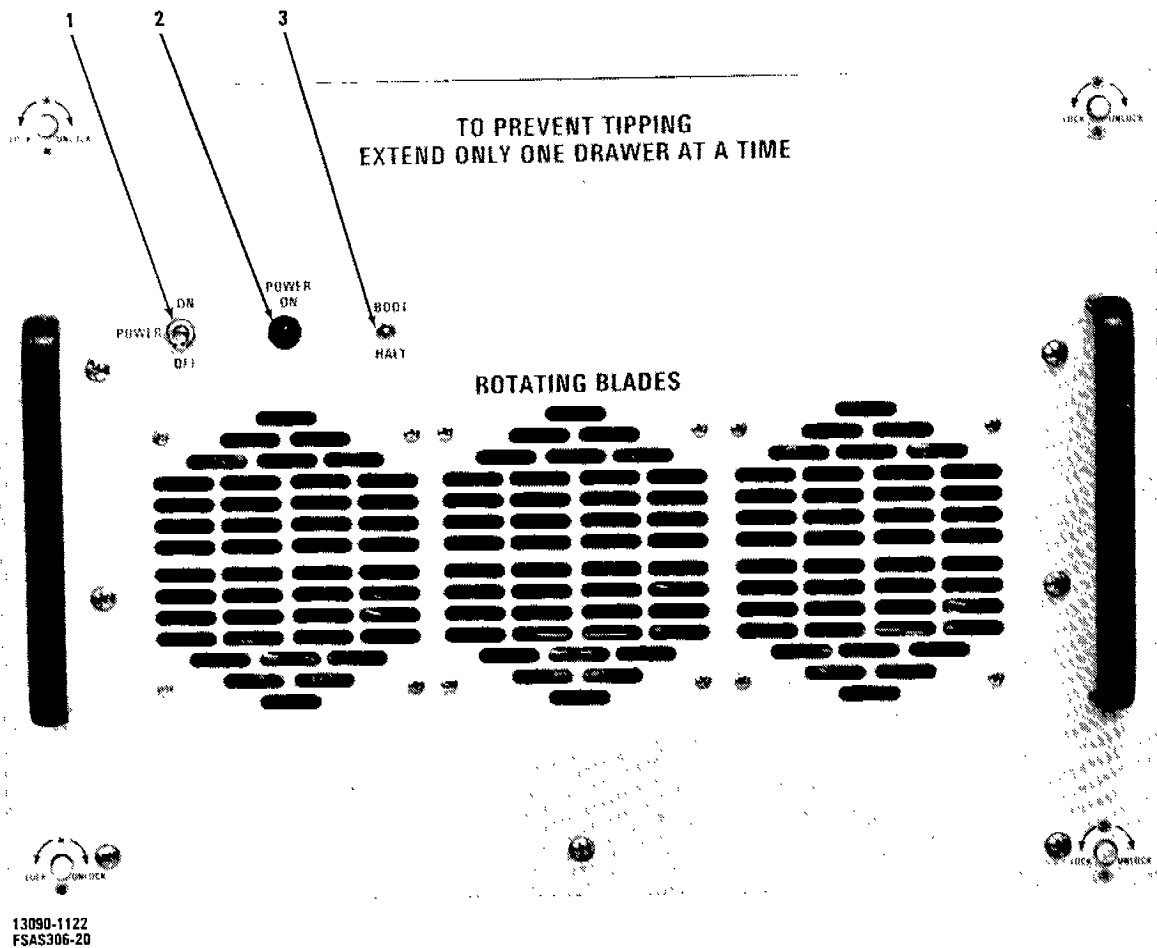


Figure 2-2. Electronics Chassis

Table 2-2

Electronics Drawer
Controls and Indicators

Fig. 2-2 Reference	Control or Indicator	Function
1	POWER ON/OFF Switch	Connects AC power to electronics chassis in ON position
2	POWER ON Indicator	Illuminates when AC power is switched through POWER ON/OFF SWITCH
3	HALT/BOOT Switch	Switch halts micro-processor activity when momentarily moved to HALT position. MADTS boot-strap sequence is initiated when switch is momentarily moved to BOOT position

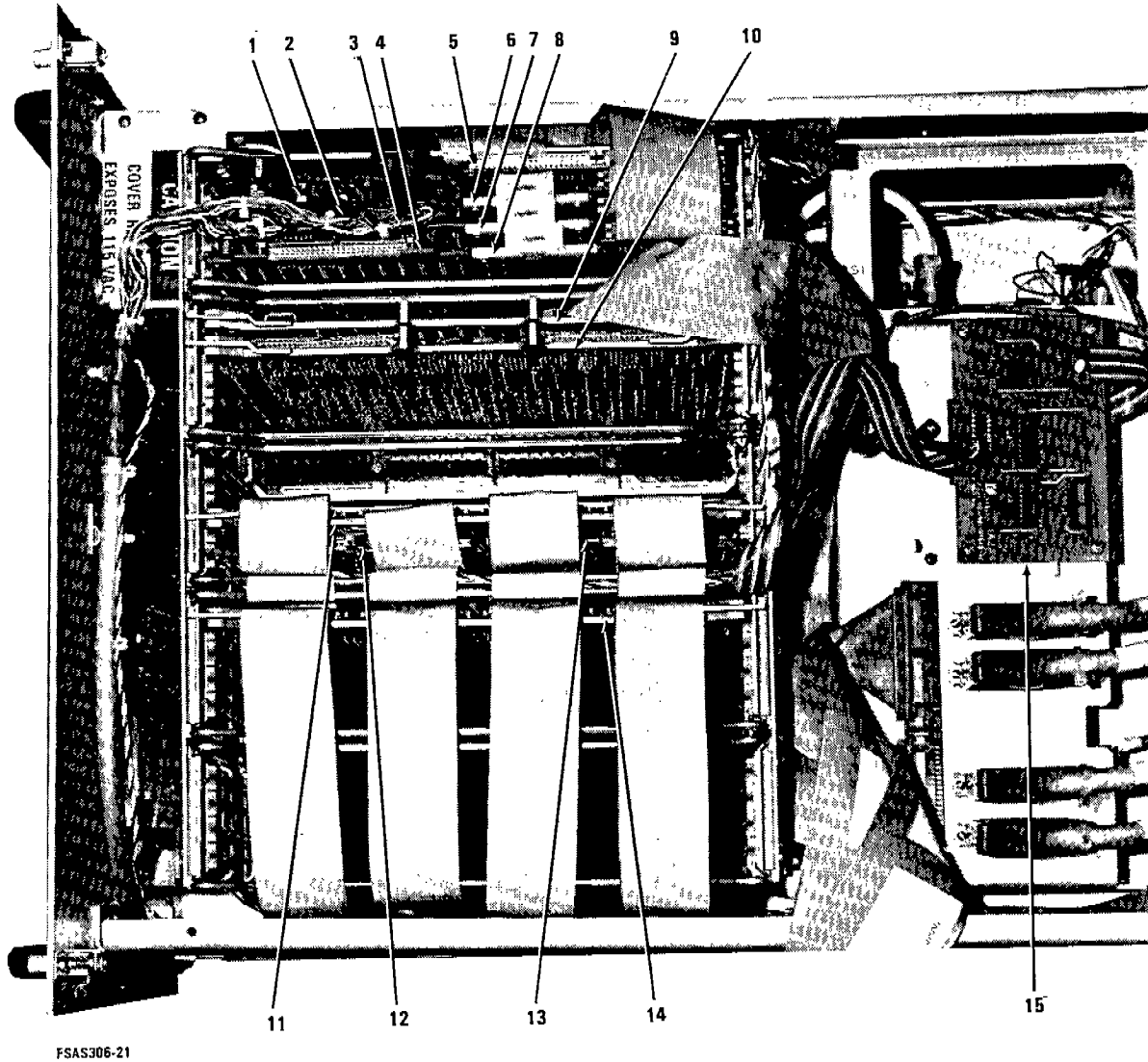


Figure 2-3. Electronics Chassis PCB Layout

Table 2-3
Electronics Chassis PCB Layout

Fig. 2-3 Reference	Reference Designator	Part/Model Number	Nomenclature
1	1A2A1A1L1	KDF11-AA	LSI 11/23 Processor (CPU)
2	1A2A1A1L2	MSV11-LF	64K Word RAM Memory/Parity
3	1A2A1A1L3	8S	8-Channel Serial I/O
4	1A2A1A1L4	DRV11-J	High Density Parallel Interface
5	1A2A1A1U1	HEX-L11	DMA 6-Channel Adapter
6	1A2A1A1U2	IPB-11	Inter-Processor Buffer
7	1A2A1A1U3	DMA-QB	DMA Controller Module
8	1A2A1A1U4	DMA-QB	DMA Controller Module
9	1A2A1A2UL1	M8061-00	Disk Controller
10	1A2A1A2UL2	401-36993-03	Multiplexer
11	1A2A1A3UL3	401-33676-01	Alphanumeric On-The-Fly Processor
12	1A2A1A3L4	KPV11-B	Power Fail-Restart Module
13	1A2A1A3U4	MRV11-C	32K Word PROM Memory
14	1A2A1A4UL1	401-33692-01	Quad Cache
15	1A2A4	401-37573-01	I/O Control Panel (PCB)
16	1PS1	MM43-12Y2Y/ 115	Power Supply

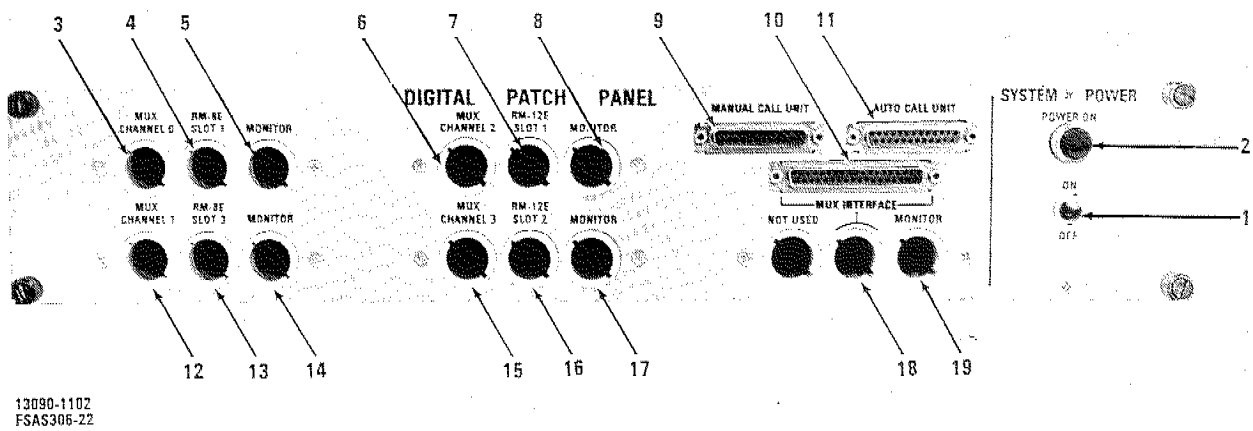


Figure 2-4. Digital Patch Panel

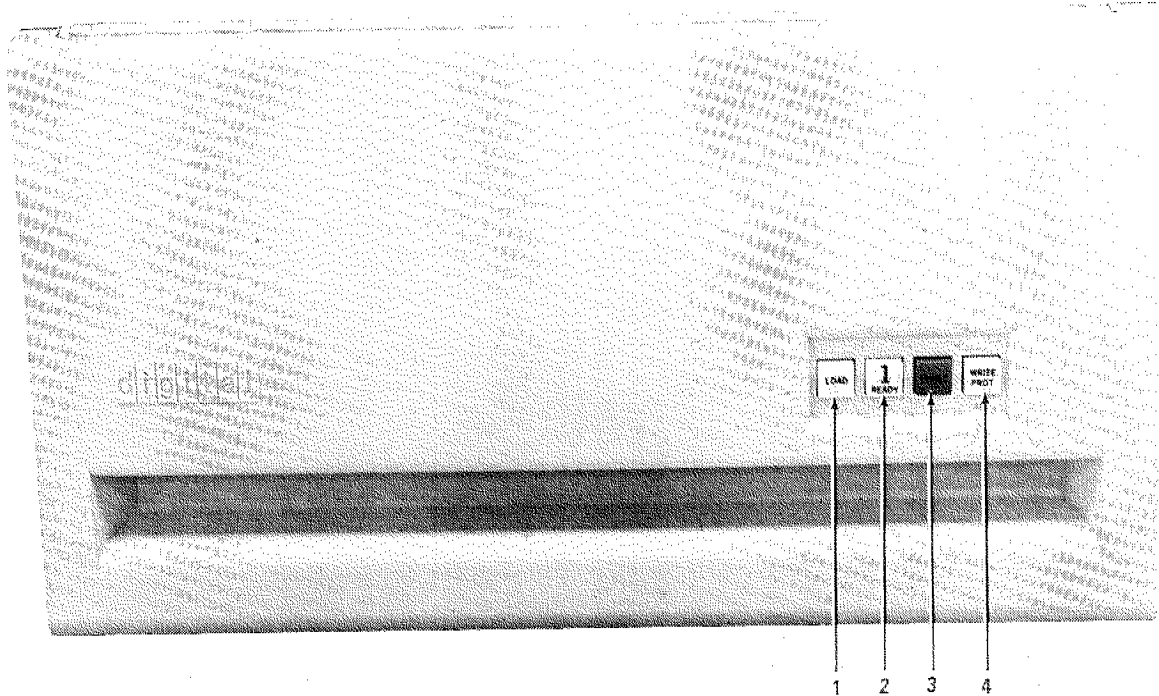
Table 2-4
Digital Patch Panel
Controls and Indicators

Fig. 2-4 Reference	Control or Indicator	Function
1	SYSTEM POWER ON/OFF Switch	Connects input AC power to MADTS rack assemblies in ON position
2	POWER ON Indicator	Illuminates when AC power is switched through SYSTEM POWER ON/OFF Switch
3	MUX CHANNEL 0	Full duplex RS-449 port for MUX CHANNEL 0
4	RM-8E SLOT 1	Full duplex RS-449 port for RM-8E SLOT 1
5	MONITOR	Monitor output not used
6	MUX CHANNEL 2	Full duplex RS-449 port for MUX CHANNEL 2
7	RM-12E SLOT 1	Full duplex RS-449 port for RM-12E SLOT 1
8	MONITOR	Monitor output not used
9	MANUAL CALL UNIT	Control input for MANUAL CALL UNIT located in RM-8E slot 0
10, 18	MUX INTERFACE	MUX INTERFACE connectors are jumpered pin-to-pin
11	AUTO CALL UNIT	Control input for AUTO CALL UNIT located in RM-12E slot 0
12	MUX CHANNEL 1	Full duplex RS-449 port for MUX CHANNEL 1
13	RM-8E SLOT 3	Full duplex RS-449 port for RM-8E SLOT 3

Table 2-4 (Continued)

Digital Patch Panel
Controls and Indicators

Fig. 2-4 Reference	Control or Indicator	Function
14	MONITOR	Monitor output not used
15	MUX CHANNEL 3	Full duplex RS-449 port for MUX CHANNEL
16	RM-12E SLOT 2	Full duplex RS-449 port for RM-12E SLOT 2
17, 19	MONITOR	Monitor outputs not used



FSAS306-23

Figure 2-5. RL01-AK/RL02-AK Disk Drive

Table 2-5

RL01/RL02 Disk Drive
Controls and Indicators

Fig. 2-5 Reference	Control or Indicator	Function
1	LOAD Switch and Indicator	<p>After LOAD Switch is depressed, the spindle motor is energized if the following conditions are met:</p> <ul style="list-style-type: none"> o RL01/RL02 cartridge is installed o cartridge protective cover is in place and cartridge access door is closed o All AC and DC voltages are within specifications o Read/write heads are retracted <p>The LOAD Indicator is illuminated if:</p> <ul style="list-style-type: none"> o Spindle motor is not energized o Spindle is stopped o Read/write heads are retracted
2	UNIT SELECT Switch and READY Indicator	<p>UNIT SELECT Switch is cam-operated and actuated by inserting the numbered, cammed button. READY Indicator illuminates approximately 45 seconds after LOAD Switch is depressed if following conditions are met:</p> <ul style="list-style-type: none"> o Read/write heads are loaded o Heads are detented on a specific track

Table 2-5 (Continued)

RL01/RL02 Disk Drive
Controls and Indicators

Fig. 2-5 Reference	Control or Indicator	Function
3	FAULT Indicator	<p>The FAULT Indicator is illuminated if any of the following errors are present:</p> <ul style="list-style-type: none"> o Drive-select error o Seek timeout error o Write current in heads error (during sector time) o Loss of system clock o Write-protect error o Write data error o Spin error
4	WRITE PROTECT Switch and Indicator	<p>WRITE PROTECT Switch is used to set or reset write protect condition. WRITE PROTECT Indicator illuminates when write protect condition is set</p>

Table 2-6

MADTS Power-Up and
Self-Test Procedures

Step #	Action	Normal Result
1.	Ensure that all circuit breakers are set to the ON position.	
2.	Connect MADTS to 115VAC 60Hz power source using AC power cable (P/N 401-37760).	
3.	Set power switch on System Power Panel to ON position.	Power indicator is lighted, outlet strip indicators are lighted, and fans operate. On disk drive, READY, FAULT, and WRITE PROTECT and LOAD indicators are lighted. Modem power supply LEDS are lighted.
4.	Set POWER switch on electronic drawer to ON position. Press disk drive load switch.	Fans in electronic chassis operate, disk drive begins to spin up. When disk is up to operating speed, FAULT, WRITE PROTECT, and LOAD lights go out and the Ready Light comes on. MADTS commences automatic confidence check, and results are printed out. After print-out is complete, it is evaluated to determine whether or not the MADTS is ready to begin troubleshooting defective assemblies.
5.	Troubleshoot defective assemblies by following procedures in the applicable section of this manual.	

SECTION III

THEORY OF OPERATION

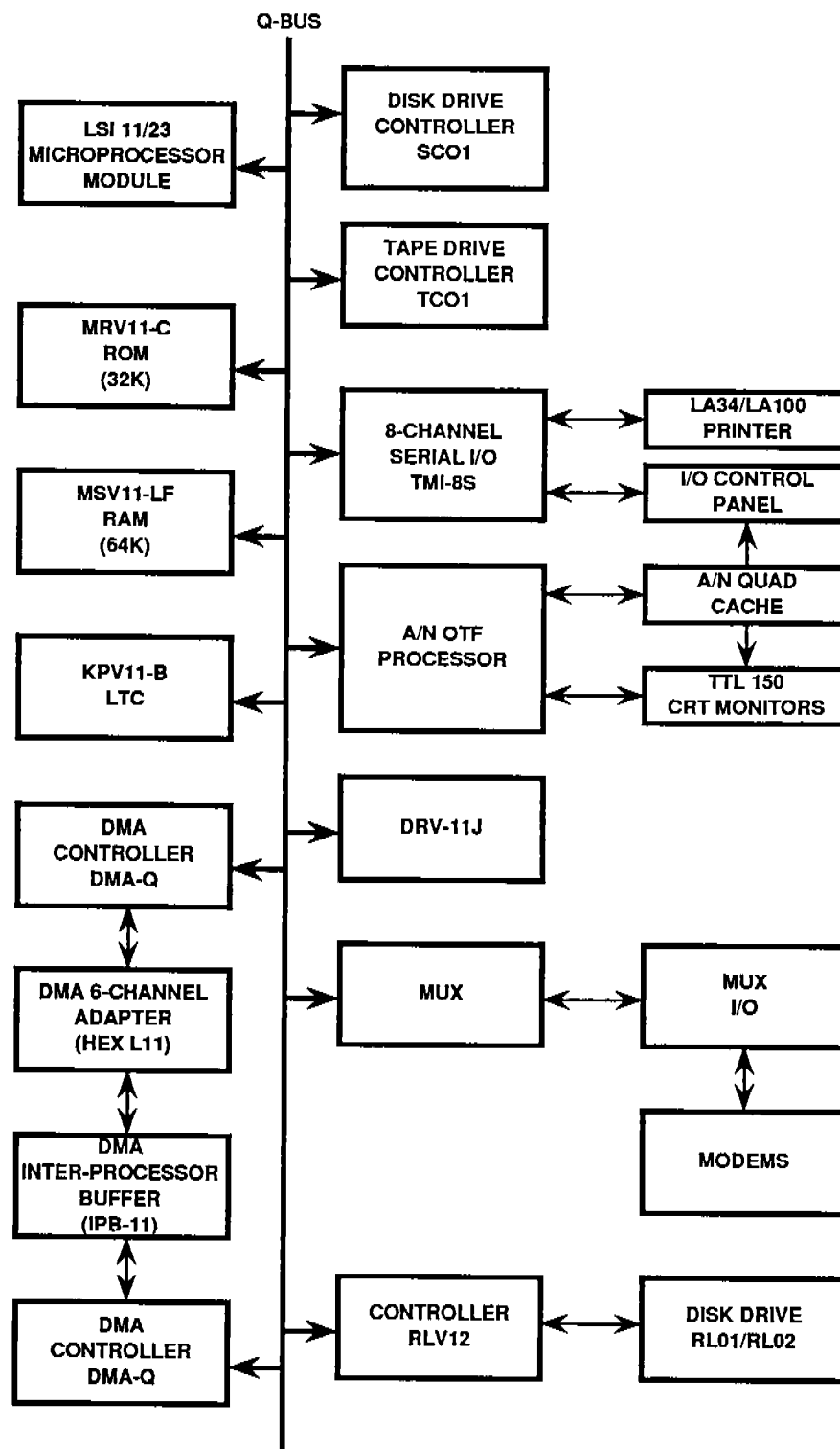
3.1 INTRODUCTION. This section contains a description of the system and functional theory of operation of the MADTS. A number of M1FC FSAS system LRUs are contained in the MADTS. A detailed theory of operation of these LRUs is not discussed in this manual, but is contained in the applicable LRU manual. A table of related LRU equipment manuals and a detailed theory of operation for the E-Systems printed circuit boards are contained in the Equipment Instruction Book, Model 1 Full Capacity Flight Service Data Processing System (TI 6490.37).

3.2 MADTS THEORY OF OPERATION. The MADTS tests LRUs by subjecting them to the same stimulus as is encountered in the on-line system operation. This type of test provides the greatest possibility for duplication of faults encountered in the system. As shown in Figure 3-1, the MADTS is configured similar to the communications processor of the AFSS.

The LSI-11/23 Processor is the CPU for the MADTS. The MRV11-C PROM board contains a self-test program for the MADTS which automatically runs at power-up or re-boot. The MSV11-LF RAM board contains 64KW of RAM, providing CPU work space and system storage. The KPV11-B is a line time clock that contains power fail and restart circuitry, as well as terminations for the Q-bus. The DMA-QB interfaces the Q-bus with other LRUs including the HEX-IPB, a microprocessor linking system. The RLV12 is a disk controller which interfaces the Q-bus to the RL01/RL02 Disk Drive. The RL01/RL02 Disk Drive contains the disk version of the LRU diagnostics for the MADTS. The 8S is an eight-port serial interface, used primarily for the LA34 or LA100 Input/Output Terminal. The E-Systems multiplexer selects the communication line being serviced. The A/N OTF processor and the QUAD Cache boards control and store the data going to the CRT display terminal.

3.2.1 System Description. The MADTS system is based on the LSI-11/23 CPU. This is the same CPU as used in the FSDPS COTC, AFSS communications processor, and AFSS position processor. The LSI-11/23 is a 16-bit high performance microprocessor with memory management. It is implemented using three chips: data, control, and memory management. The data chip performs all arithmetic and logical functions, handles data and address transfers, and coordinates most interchip communication. The control chip provides microprogram sequencing for instruction decoding and contains the control store ROM. The memory management chip contains the registers for 18-bit memory addressing, floating point registers, and accumulators.

The microprocessor communicates with memory and other peripheral circuitry via the Q-bus. Figure 3-1 is the MADTS block diagram showing the processor, Q-bus and LRUs on the Q-bus.



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Figure 3-1. MADTS Block Diagram

Memory for the microprocessor is contained on the MRV11-C 32K PROM board and the MSV11-LF 64K RAM board. The MRV11-C is a high density ROM module designed for use with the LSI-11 bus and configured for 32K of ROM. The ROM is used for additional instruction codes and other dedicated memory applications. The MSV11-LF random access memory is a volatile memory array designed for use with the LSI-11 bus, and contains 18 64Kx1-bit storage chips. This array supplies a refresh circuit, and the memory storage is used generally for scratch pad and other types of work space.

The KPV11-B is an LRU which operates with the LSI-11/23 through the Q-bus to provide power-up sequence signals, and a line time clock. The KPV11-B also provides 120 ohm termination for Q-bus lines.

The HEX-IPB is a high-speed interface that allows data transfer between a host processor and one of six satellite computers. The interface consists of two boards, the HEX board and the IPB board. The HEX board has six 40-pin sockets with tri-state buffers to provide the one-of-six selection to the IPB. The IPB (inter-processor buffer) has a 40-pin connector to connect to the host, and provides programmed I/O communication between the host and selected satellite.

The DMA-Q is a general purpose direct-memory access that allows devices to be interfaced to the Q-bus. The DMA-Q supplies interface protocol, can access extended memory, and can interrupt on one of four different levels. A provision for user-supplied PROM is provided on the board.

The 8S board is a Q-bus compatible interface board containing eight full-duplex serial I/O ports. Each port may be independently configured for RS-232C, RS-422, or RS-423. Baud rates may be independently selected from 75 to 153.6K baud. Other selections are: number of data bits; number of stop bits, parity checking, and parity sense.

The RLV12 Disk Controller is the interface for the RL01/RL02 Disk Drive to the LSI-11 Q-bus. The controller is contained on a single quad-size pcb. It can support up to four disk drives, and is capable of DMA operations with the Q-bus. DMA data transfer rates of 200K words per second are possible with the RLV12.

The E-Systems multiplexer is a four-channel serial communications processor designed to interface the LSI-11 Q-bus with other device communications. The multiplexer has an on-board microprocessor which makes the required logical decisions and controls the data transfers that it handles. Each channel is a full duplex RS-449 port, capable of operation in asynchronous, bit synchronous, or byte synchronous modes. The multiplexer has a self-test capability with test results indicated on a series of LEDs, eight red LEDs and one

green LED. The self-test is initiated when power is first applied, or by a command from the LSI-11. The green LED is illuminated when the self-test is successfully completed. An error code is displayed on the red LEDs if the test detected a malfunction.

The Alphanumeric On-The-Fly (A/N OTF) Processor functions as a controller for the Quad Cache board and associated display terminals. The A/N OTF processor receives and decodes address and data bits via the Q-bus. If the processor is selected, it enables selection of the Quad Cache board, and one of the display monitors. The A/N OTF contains 3 E-Systems Pico Processors (EPPs) which generate control signals and addresses for internal use, and on the Quad Cache board.

The Quad Cache memory board contains memory for four display terminals. Each individual cache contains 2K words of storage. Data from the A/N OTF processor is transferred to the selected display monitor, on command from the processor. The cache contains refresh circuitry and works on a hand-shake basis with the A/N OTF processor to provide data to the display terminals.

The RL01/RL02 Disk Drive is a mass storage system employing a magnetic disk cartridge as the storage medium. The drive is contained in a chassis that slides out of a mounting rack for access to the magnetic disk cartridge. The chassis may be removed from the rack for servicing. The chassis contains the drive mechanism, read/write heads, power supply, air supply system, logic modules, interlocks, and connectors for I/O cables. The RL01/RL02 disk cartridge contains a single platter for data storage using both sides of the platter. The RL01 disk cartridge has a capacity of 5.2 megabytes. The RL02 disk cartridge has a capacity of 10.4 megabytes.

The TTL 150 CRT Monitor is used at a data terminal with keyboard input logic. It accepts three TTL compatible direct drive input signals. These signals are the video, or data information, the horizontal sync, and the vertical sync. The monitor has a 15 inch CRT and 110 degree deflection. Brightness power and contrast controls are located on the front panel to turn the monitor on and adjust the display intensity of the green phosphor of the CRT.

The RM-8E Modem Enclosure has redundant power supplies and contains mounting slots for eight PC modem cards. These power supplies are chassis mounted and removable from the front of the enclosure. They are continuously monitored, and out-of-tolerance conditions are reported by a flashing front panel LED. When an improper operation is detected, the failed power supply is automatically disconnected, and the standby power connected to provide modem power. The rear panel contains telephone and data terminal interface equipment connectors for eight modems, and a manual call unit. The front

panel is hinged to open for access to component assemblies. The panel contains translucent windows to enable monitoring of the LEDs on the front edge of each assembly. PC cards usable in the RM-8E include:

- RM-208A
- RM-9600
- RM-A/O
- RM-800
- RM-9600E FP

The RM-208A is a stand-alone 4800 bps modem when used on a 4-wire lease line, or it may be used on a dial-up network with an RM-A/O. The RM-9600 and RM-9600E FP modems are 9600 bps modems with provisions for 2400 and 4800 bps operation. The RM-9600 is stand-alone and operates only on a 4-wire lease line. The RM-A/O is a pc board which converts a 208A modem from 4-wire private line use to 4-wire dial-up. The A/O allows automatic answer on two dial-up lines, or manual call-out on two dial-up lines (when used in conjunction with the RM-800). The RM-800 is a manual call unit which allows manual call-out on the RM-208A line. The RM-800 must be in slot 0 of the housing when in use.

The LA34/LA100 is a microprocessor based, desk top I/O terminal capable of print speeds up to 45 characters per second. The terminal prints characters by the dot matrix method. It has a typewriter-style keyboard which includes the printer control for the terminal. The LA34/LA100 is used as a maintenance terminal.

The MUX Interface assembly adapts two 50-pin ribbon cables from the multiplexer to four 37-pin D-type connectors. This allows conformance to RS-449. Signal level generators are supplied on the interface which provide signal levels to unused connections in the RS-449 interfaces.

The Coded Time Source (CTS) Interface receives and compares time data from two individual CTS units. The data is serialized for input to a Tandem asynchronous port. The CTS Interface provides a Time/Days counter to supply the correct time and day of the year. If a time error is detected, the error indicator is illuminated.

The Kennedy model 9000 is a synchronous digital, magnetic tape drive unit, providing high reliability at moderate speeds. With proper external format control, it will read and write IBM-compatible tapes. The tape drive is equipped with the electronics for reading and writing tapes, and controlling tape motion. However, formatting, parity generation, and other data requirements are not included, and must be provided in order to generate properly formatted, IBM compatible tapes. The tape is recorded in 7 or 9 track NRZI, or 9 track phase encoded, with densities of 200-1600 cpi. The standard tape speed is 25 ips; however, speeds from 10-45 ips may be obtained. The data transfer rate at 25 ips, 800 cpi, is 25 kHz.

The Ampex DM9300TD dual-port disk drive is a self-contained, single-spindle, direct-access device. The drive uses an IBM 3336 Model 11 twenty-surface disk pack, or equivalent. Each pack has 19 data surfaces with one surface reserved for pre-recorded servo, positioning, and track-to-track information. The data capacity of the pack used in the DM9300TD is 300 million eight-bit bytes. The dual-port design enables two controllers to be connected to the drive, allowing each controller full access to the drive when it is not busy with the other controller. The drive has a linear DC motor, and a linear positioning motor that positions the heads, carriage, and head assembly. Blowers circulate filtered cooling air throughout the drive. Disk packs are installed and removed through the front-loading shroud area, accessible when the hinged front cover opens after the pack comes to a stop.

The E-Systems keyboard is the input device for operator terminals of the AFSS. The keyboard is a 96 keyswitch matrix constructed on a pcb which contains a microprocessor to decode the key-stroke inputs. The keyboard is powered by a modular +5 VDC power supply which uses 110 VAC for primary power. The keyboard is housed in a metal chassis and cover, with power and data connectors, and a reset switch located on the rear panel. The reset switch is used for recycling the microprocessor in the event that a lock-up occurs.

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 GENERAL. This section contains maintenance instructions for the MADTS. The maintenance activities consist of both preventive and corrective maintenance. Procedures for both types of maintenance are provided in this section, including maintenance schedules when scheduled maintenance is part of the maintenance program.

4.2 PREVENTIVE MAINTENANCE. Preventive maintenance for the MADTS consists of inspection, cleaning, and performance evaluation of the self-test (automatic confidence check). A schedule for preventive maintenance activities is given in Table 4-1.

4.2.1 Inspection. Inspection includes, but is not limited to, visual checks for cracked or broken indicator lenses, broken knobs, loose or broken switches, bent or broken connector pins or housings, missing hardware, sticking or inoperative drawer slides, and cracked or bent structural parts. Also, check wiring for frayed, brittle, or missing insulation, broken wires, proper strain relief, and cable identification markers. For individual equipment refer to the M1FC FSAS System Instruction Book TI 6490.36.

4.2.2 Cleaning. Cleaning the MADTS generally consists of removal of accumulated foreign matter such as dust, lint, and dirt. Front panels should be wiped clean daily. Interiors of drawers and rear of the rack should be cleaned weekly by use of low pressure air to blow dirt away, or a vacuum cleaner with a bristled nozzle. For individual equipment refer to the M1FC FSAS System Instruction Book TI 6490.36.

4.2.3 Self-Test. Self-Test for the MADTS consists of performing the automatic confidence check and verifying its completion with no faults. The self-test is initiated each time the MADTS is powered up, or it may be invoked by operating the RE-BOOT switch on the electronics drawer, or by a software command. The message results of the confidence check determines if further tests are necessary. For a detailed explanation of the confidence check and message, see Section VII.

4.3 CORRECTIVE MAINTENANCE. Corrective maintenance for the MADTS comprises replacement of LRUs or other items having been identified as failed or faulty. Once an assembly or item has been identified as failed or faulty, refer to the appropriate procedure in this section for the instructions to remove and replace the assembly or item identified.

4.4 REMOVAL AND REPLACEMENT. The following paragraphs contain the procedures for removal and replacement of assemblies that may be removed at maintenance levels other than depot. After removal and replacement of an assembly, run the confidence check to ensure that

the fault has been removed. If not, analyze the confidence check message for an indication of what the problem is, and proceed to troubleshooting.

4.5 REMOVAL AND REPLACEMENT, MODEM ENCLOSURE RM-8E. The following procedure contains instructions for removal and replacement of the RM-8E Modem Enclosure of the MADTS. The MADTS contains two modem units, and these instructions apply equally to either of them.

- a. Disconnect all data connectors from rear panel of RM-8E.
- b. Disconnect power cord of RM-8E from power outlet.
- c. Remove all modem cards from enclosure.
- d. Remove form screws securing enclosure to rack, and slide enclosure out through front of rack.
- e. Replace by reversing steps of this procedure.

4.6 REMOVAL AND REPLACEMENT, CRT DISPLAY TTL-150. The following procedure contains instructions for removal and replacement of the TTL-150 CRT Display, which is mounted in the MADTS rack.

- a. Disconnect all coaxial connectors from rear panel of display.
- b. Disconnect AC power cord of display from power outlet.
- c. Remove four cross-point screws securing mounting bracket and display to MADTS rack, and slide display out through front of rack.
- d. Reverse removal steps to replace display.

4.7 REMOVAL AND REPLACEMENT, MADTS CONTROL PANEL. This procedure contains instructions for removal and replacement of the MADTS I/O control panel.

- a. Remove all connectors from front and rear panels of I/O control panel.
- b. Loosen four captive screws securing control panel to rack.
- c. Slide control panel out through front of rack.
- d. Reverse removal procedure to replace control panel.

4.8 REMOVAL AND REPLACEMENT, ELECTRONICS DRAWER. This procedure contains the instructions for removal and replacement of the electronics drawer assembly.

CAUTION

The electronics drawer weighs approximately 50 lbs. and should be handled by two persons.

Table 4-1
Preventive Maintenance Schedule

Activity	Frequency
Inspection	D
Cleaning	D, W, M
Self-Test	D

D = DAILY, W = WEEKLY, M = MONTHLY

- a. Disconnect all cables on rear panel of drawer, and loosen nut to remove bolt holding ground strap to drawer.
- b. Slide drawer out of rack on slides until stop is reached.
- c. Release slide stops simultaneously and pull drawer out.
- d. Reverse removal steps to replace electronic drawer.

4.9 REMOVAL AND REPLACEMENT, ELECTRONICS DRAWER POWER SUPPLY. This procedure contains instructions for removal and replacement of the power supply in the electronics drawer.

- a. Pull electronics drawer out on slides until catches on slide mechanism engage and hold drawer stationary.
- b. Locate opening on left side of electronic drawer chassis which exposes terminal panel of power supply. Remove each wire and tag for identification.
- c. Loosen and remove four nuts on bottom of electronics drawer chassis. Remove two bolts extending through power supply chassis, and electronics drawer chassis, just below terminal panel.
- d. Slide power supply to left while supporting it through bottom opening in electronics drawer chassis. Remove power supply to bench.
- e. Reverse removal procedure to replace power supply.

4.10 REMOVAL AND REPLACEMENT, RL01/RL02 DISK DRIVE. The following procedure contains instructions for removal and replacement of the RL01/RL02 Disk Drive as installed in the MADTS rack.

CAUTION

The RL01/RL02 Disk Drive weighs approximately 75 lbs. and should be handled by two persons.

- a. Extend disk drive forward on rails to its farthest extension.
- b. Disconnect all connecting cables.
- c. Remove four screws securing RL01/RL02 rails to rack-mount rails. Two rear-most screws should be accessible through openings in rack-mount rails.
- d. Lift stops on each rail and slide RL01/RL02 out.
- e. To replace RL01/RL02, reverse removal steps.

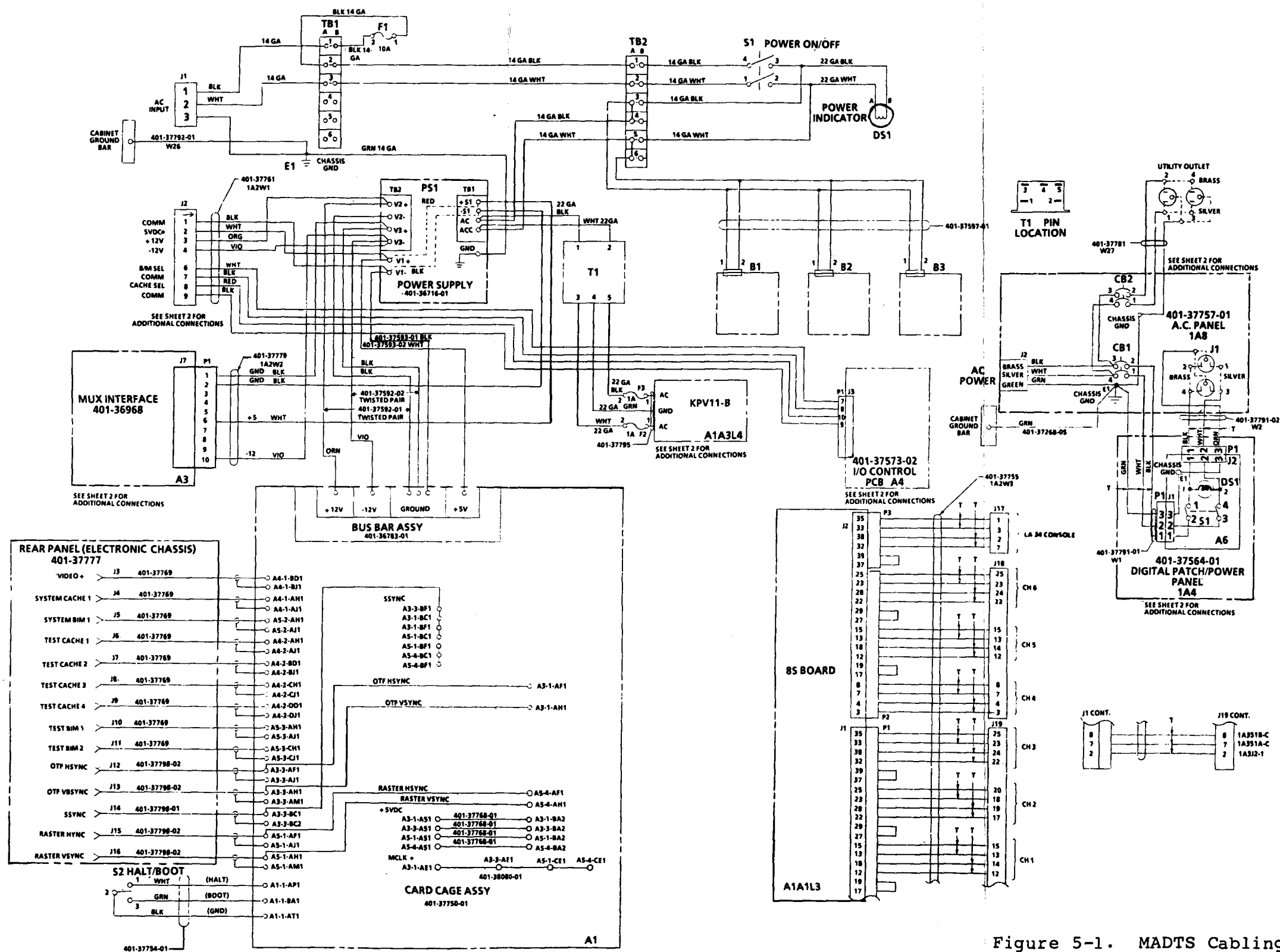
SECTION V

DIAGRAMS

5.1 MADTS DIAGRAMS. This section contains cabling diagrams and E-System schematic drawings for use as maintenance aids. Refer to the Model 1 Full Capacity Flight Service Data Processing System Equipment Instruction Book (TI 6490.37) for the table of related LRU equipment manuals. Refer to Table 5-1 for the index of MADTS diagrams.

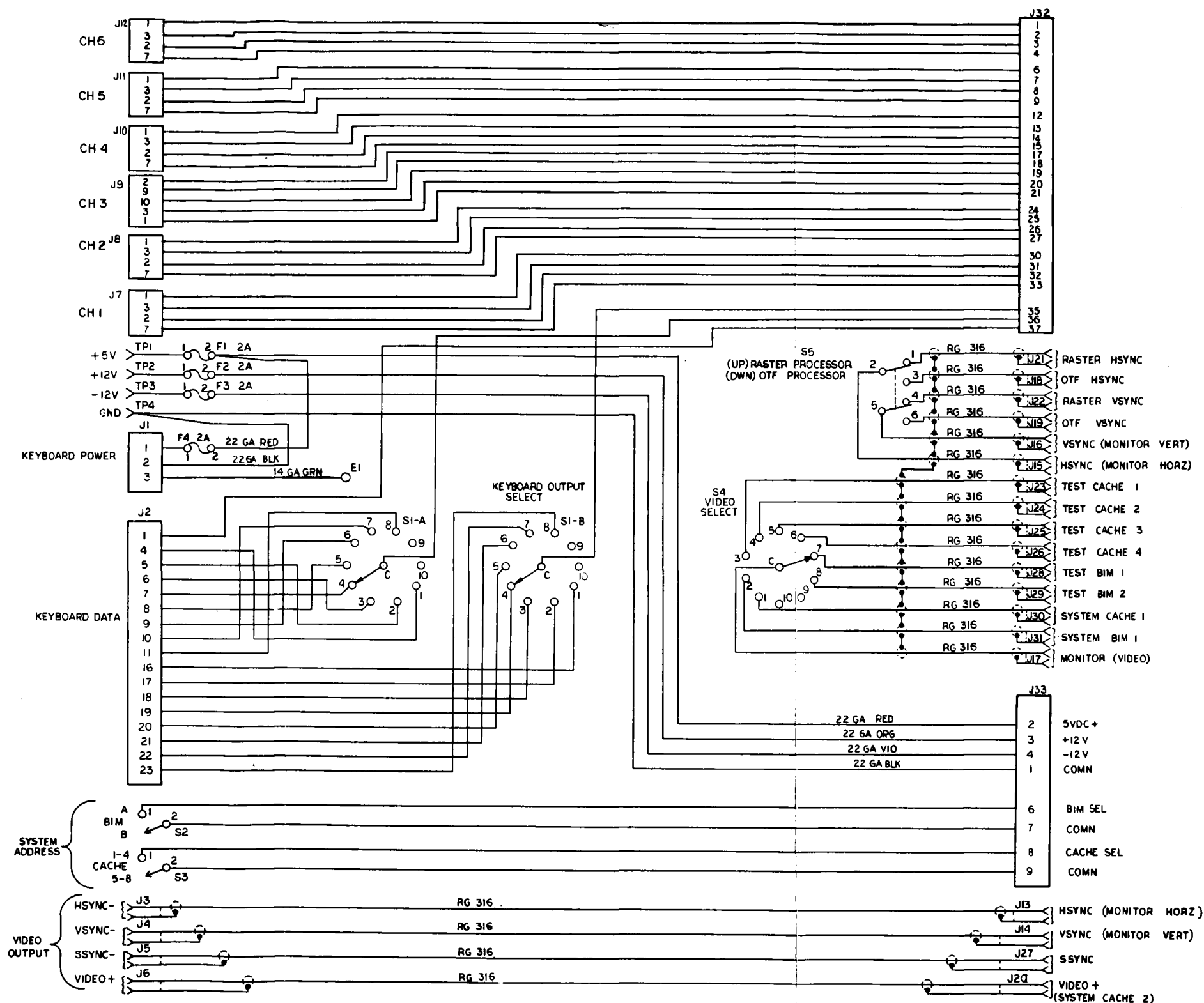
Table 5-1
Index of Diagrams

<u>Figure Number</u>	<u>Title</u>	<u>Page</u>
5-1	MADTS, 401-37570, Cabling Diagram	5-3
5-2	MADTS I/O Control Panel, 401-37575, Wiring Diagram	5-7
5-3	MADTS I/O Control Board, 401-37573, Schematic Diagram	5-9



REFERENCE DESIGNATORS ON THIS SHEET ARE ABBREVIATED.
PRECED EACH WITH 1A2. EXCEPT 1A4&1A8

Figure 5-1. MADTS Cabling Diagram
(Sheet 1 of 2)



401-37579/2 REV B

Figure 5-2. MADTS I/O Control Panel Wiring Diagram

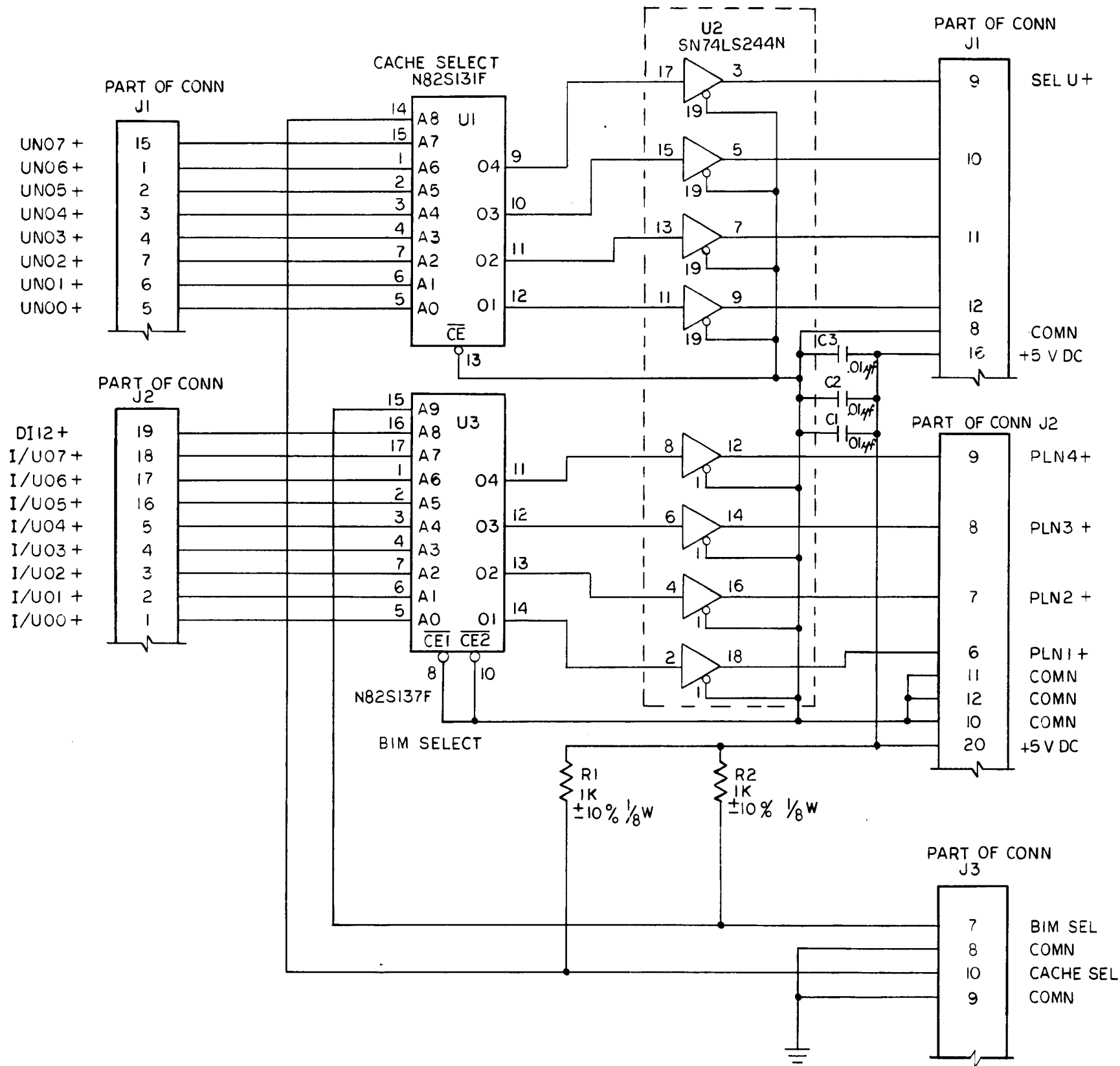


Figure 5-3. MADTS I/O Control Board Schematic Diagram

SECTION VI

MADTS PARTS LIST

6.1 GENERAL. This section contains the MADTS parts list. Only those parts peculiar to the MADTS are included.

6.1.1 Parts List Configuration. Indenture levels are used in this parts list to show the relation of a line item to the end item. A letter inserted in this block illustrates a lateral and descending "family tree" relationship of each line item to and within the end item and its discrete components (units), assemblies and subassemblies, and sub-subassemblies.

6.2 Parts List. The parts list for MADTS is given in Table 6-1.

TABLE 6-1
PARTS LIST, MADTS

INDENT	REF DES	NOMENCLATURE	PART NO.
A		MAINTENANCE AND DIAGNOSTIC TEST SET (MADTS)	401-37570-01
B	UNIT 1	MADTS RACK ASSEMBLY	401-37571-01
C	1A1	DISK DRIVE	RL01-AK/RL02-AK
C	1A2	ELECTRONICS CHASSIS	401-36720-03
C		CHASSIS SUBASSEMBLY	401-36722-02
C		FRONT PANEL	401-37776-01
C		POWER SUPPLY ASSEMBLY	401-36716-01
C		CABLE ASSY, COAX VIDEO INTERFACE	401-37769-01
C		REAR PANEL FRAME	401-36724-01
C		CARD CAGE ASSEMBLY	401-37750-01
C		AC WIRING HARNESS MADTS	401-37596-01
C		ACCESS PANEL	401-36727-01
C		CABLE ASSEMBLY, COAX INTERFACE	401-37798-01
C		CABLE ASSEMBLY, COAX INTERFACE	401-37798-02
C		TRANSFORMER	241-4-24
C		MUX INTERFACE/I/O CB ASSEMBLY	401-37764-01
C	1A2W3	CABLE ASSEMBLY, SERIAL I/O, SIGNAL	401-37755-01
C	1A2W2	CABLE ASSEMBLY MUX INTERFACE	401-37779-01
C	1A2W1	CABLE ASSY POWER I/O CONTROL PCB	401-37761-01
C		REAR PANEL	401-37777-01
C	1A2W4- 1A2W7	CABLE ASSEMBLY MUX INTERFACE SIG. OUTPUT	401-37780-01
C		CLAMP	155-8586-001

TABLE 6-1
PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
B		RM-208A MODEM	2082278
B		RM-A/O AUTO CALL/AUTO ANSWER UNIT	1020364
B		RM-800 MANUAL CALL UP UNIT	1020377
B		CABLE ASSY (RL01/RL02 DISK DRIVE)	BC06R-06
B	1A2W8	CABLE ASSY, SIGNAL, DISK DRIVE	401-3778-01
B	1A2W24	CABLE ASSY, UNIT SELECT	401-37782-01
B	1A2A1A2L3	BUS GRANT JUMPER, WITH DIODE	401-37909-09
B	1A2A1A2U3; U4;L4	BUS GRANT JUMPER	401-37909-10
B	1A2W9, 1A2W10	CABLE ASSY, MUX INTERFACE	401-37759-01
B	1A2W3	CABLE ASSY, SIGNAL, SERIAL I/O	401-37755-01
B		24V-AC, POWER HARNESS	401-37795-01
B	1A2A1A1L1	LSI-11/23 PROCESSOR M8186	KDF11-AA
B	1A2A1A1L4	4 CHANNEL PARALLEL INTERFACE	DRV11-J
B	1A2A1A1LU	MEMORY, RAM(64KW) (M8059)	MSV11-LF
B	1A2A1A3L4	POWER FAIL/RESTART (M8016)	KPV11-B
B	1A2A1A3U4	MEMORY, PROM(32KW) (M8048)	MRV11-C
B	1A2A1A2UL1	RLV12 CONTROLLER, DISK	M8061-00
B	1A2A1A1U1	6 CHANNEL INTERFACE	HEX-L11
B	1A2A1A1U2	DMA INTER-PROCESS BUFF	IPB-L11
B	1A2A1A1U3 1A2A1A1U4	DIRECT MEMORY ACCESS CONTROLLER SET (MADTS), MODEL I	DMA-QB
B	1A2A1A1L3	8-PORT SERIAL I/O INTERFACE	8S
B	1A2A1A1UL2	4-CHANNEL MULTIPLEXER	401-36993-03

TABLE 6-1
PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
B	U93	OPTION PLUG	401-37124-01
B		DISK CONTROLLER	SC01/B1
B		PROM SET (SC01-B1-RECURRING	AM2765185DC
B		TC01 LSI 11 TAPE CONTROLLER	TC01/P
B	1A2A1A3UL3	OTF PROCESSOR	401-33676-01
B		PROM SET (FOR MRV11-C BOARD	401-37747-03
B	U60 (OTF)	PROG. PROM	316-3017-001
B	1A2A1A4UL1	QUAD CACHE	401-33692-01
B	1A2W11 1A2W12	DMA INTERFACE CABLE ASSY	401-37767-01
B	1A2W13 thur 1A2W22	RIBBON CABLE ASSY	401-37762-01
B		CABLE ASSY, TEST, CTS, CLOCK NO. 2	401-37876-01
B		CABLE ASSY, SERIAL I/O (LA34)	401-37126-07
B		MUX I/O CABLE	401-37142-02
B		CABLE ASSY, POWER, MUX	401-37739-01
B		CABLE ASSY, TEST, KENNEDY TAPE DRIVE, CONTROL	401-37845-01
B		CABLE ASSY, TEST, KENNEDY TAPE DRIVE, DATA	401-37846-01
B		CABLE ASSY, TEST, AMPEX DISK DRIVE, DATA	401-37847-01
B		CABLE ASSY, TEST, AMPEX DISK DRIVE, CONTROL	401-37848-01
B		CABLE ASSY, TEST, CTS, CLOCK NO. 1	401-37849-01
B		CABLE ASSY, TEST, LOOP BACK, 4 POSITION	401-36863-01

TABLE 6-1

PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
B		CABLE ASSY, TEST, LOOP BACK, 3 POSITION	401-37864-01
B		CABLE ASSY, KENNEDY TAPE DRIVE, LOOP BACK	401-37872-01
B		CABLE ASSY, TEST, MUX INTERFACE	401-37881-01
B		CABLE ASSY, TEST, POWER, KEYBOARD	401-37865-01
B		CABLE, KEYBOARD INTERCONNECT	401-37738-11
B		CABLE, VIDEO	401-36797-02
B		32 CIRCUIT PATCH CORD	DPC-32-3
B		EXTENDER BOARD (FULL SLOT)	W987-00
B		EXTENDER BOARD (HALF SLOT)	W984-00
C		DISK PACK	RL01K-DC
C	1A6	MODEM ENCLOSURE, RM-8E	52005060
C	1A7	MODEM ENCLOSURE, RM-12E	51020362
C	1A4	DIGITAL PATCH PANEL	401-37564-01
D		CABLE TIE	TY524M
D		CONNECTOR CONTACT (SOCKET)	350550-1
C	J1 AND J2	CONNECTOR HOUSING CAP	350767-1
C		TERMINAL	RB250
C		PANEL	401-37844-01
C		COVER	401-37867-01
C		CHASSIS	401-37866-01
D		CONTACT PIN	350547-1
C	XDS1	LAMPHOLDER	DLO-61B-DO6 BGT

TABLE 6-1
PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
C	S1	SWITCH	7599K1
C		DYNA-PATCH JACK	DP-32-5
C	DS1	LAMP	CL24-120PS
C		MARKER KIT	401-37796-01
C	1A5	MONITOR ASSY	401-37566-01
C	1A3	I/O CONTROL PANEL ASSY	401-37575-01
D	J3-J6, J13, J31	BNC CONNECTOR	31-10
D		JACKPOST KIT	D20418-2
C	SPARE	FUSEHOLDER	FHL17G1
C	J32	CONNECTOR	DCMA-37S
C	XF2, XF3	FUSEHOLDER	FHL18G1-1
C	JACK, RED	INSULATED BANANA	1509-102
C	JACK, BLK	INSULATED BANANA	1509-103
C	JACK, GRN	INSULATED BANANA	1509-106
C	JACK, PUR	INSULATED BANANA	1509-112
C	FEM J1	CONNECTOR CONTACT	350550-1
C	J33	CONNECTOR HOUSING	350782-01
C	J7-J12	CONNECTOR	DBMA25S
C	XF1, XF4	FUSEHOLDER	FHL18G1-8
C	F1-F4 & SPARE	FUSE, 2 AMP	312002
C	J2	CONNECTOR	552840-1
C	J1	CONNECTOR HOUSING	350767-1
C		JACKPOST KIT	552568-1

TABLE 6-1
PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
C	FEM J1 & J33	CONTACT CONNECTOR	350689-1
D		SHRINK TUBING	M23053/ 5-106-0
D		RING LUG	MS25036-108
D		SHRINK TUBING	M23053/ 5-104-0
D		RING LUG	MS25036-108
D		SHRINK TUBING	M23053/ 5-104-0
D		CABLE TIE	TY524M
D		SOLDER SLEEVE	M83519/1-3
D		SOLDER SLEEVE	M83519/2-8
C	1A8	AC J-BOX	401-37757-01
C	OR EQ	RAISED COVER	52-C-16
C	OR EQ	UTILITY BOX COVER	58-C-7
C	OR EQ	CONNECTOR, UTILITY	5362-1
C	OR EQ	CONNECTOR/INPUT	2615
C	OR EQ	UTILITY BOX COVER	52C1
C		CABLE ASSEMBLY, UTILITY	401-37781-01
D		TERMINAL (AWG 14 #8)	MS25036-153
C		CABLE ASSEMBLY, SYSTEM POWER	401-37791-01
C		CABLE ASSEMBLY, SYSTEM POWER	401-37791-02
C		CABLE ASSEMBLY, GND STRAP	401-37268-08
C		TERMINAL (AWG 14 #6)	MS25036-106

TABLE 6-1

PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
C		SHRINK TUBING	M23053/ 5-114-0
C		PANEL	401-37765-01
C	S1	SWITCH	71AD36-020-1- AJUN
C	S4	SWITCH	71AD36-01-1- AJUN
C	S2, S3	SWITCH	TT13A-3T
C	S5	SWITCH	7201
C		KNOB	33-12BLK
C	CB1, CB2	CIRCUIT BREAKER	JA2-T3-A-20-2
C	W3	CABLE ASSY, AC PWR	401-37760-01
C	W20	CABLE ASSY, CHANNEL SELECT	401-37756-01
C	W19	CABLE ASSY, I/O CONTROL PANEL PWR	401-37758-01
C	W15 THRU W18	CABLE ASSY, COAX VIDEO	401-37766-01
C	W21 THRU W25	CABLE ASSY, COAX VIDEO	401-37766-02
C	XF1, XF2 XF3	FUSEHOLDER	FHL17G1
C		HANDLE	164-0193-001
C		WIRING HARNESS, HALT/BOOT	401-37754-01
C		24V-AC POWER HARNESS	401-37795-01
C		SLIDE	1504639-L
C		SLIDE	154639-R
C	DSI	LAMP	CL24-120PS
C	XDSI	LAMPHOLDER W/LENS	DLO-61B-D06BGT

TABLE 6-1

PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
C		COVER, AC	401-37783-01
C		COVER, TERMINAL BLOCK	401-37784-01
C	B1, B2, & B3	FAN	WR2H1
C	F2 & F3 SPARE	FUSE, 1 AMP	312001
C	F1 SPARE	FUSE, 10 AMP	312010
C		SADDLE SUPPORT BASE	TC 142
C		NAMEPLATE (ESY)	401-37771-02
C		NAMEPLATE, ELECTRONIC CHASSIS	401-38076-01
C		NAMEPLATE, (FAA)	401-37772-01
C		GUIDE, RECEPTACLE	12-11591-38
C	W39	CABLE ASSY-COMMUNICATIONS	401-37273-27
C	1A9 and 1A10	OUTLET STRIP	UL24CB-6
C	W29 thru W32	CABLE-ASSY COMMUNICATIONS	401-37273-22
C	W26	CABLE ASY-GND.-ELECT. CHASSIS	401-37792-01
C		CARD, EDGE-ZIF RECEPTACLE	12-11591-35
C		GRIP LATCH	43-10-1-0
C		RM-8E POWER SUPPLY	51020249
C	1A2W8	CABLE ASSY, DISK DRIVE, SIGNAL	401-37778-01
C		MOUNTING CLIP	477663
C		MOUNTING PLATE	TC105A
C		RM-12E POWER SUPPLY	52002272
C		PHONE LINE LOOP BACK	401-37906-01

TABLE 6-1
PARTS LIST, MADTS (CONT'D)

INDENT	REF DES	NOMENCLATURE	PART NO.
C	W33, W34	CABLE ASSY, COMMUNICATIONS	401-37273-23
C	W35 thru W38	CABLE ASSY, COMMUNICATIONS	401-37273-19
C		CABLE ASSY, SERIAL I/O	401-37126-17
C		JACK ARRANGEMENT (MALE)	131SB15DS-006
B	UNIT 2	LA34-AA/LA100-CA PRINTER	LA34-AA/LA100-CA
B		TRACTOR FEED (PRINTER)	LA10X-AL
B		STAND (PRINTER)	LAX34-SL

SECTION VII

GENERAL INFORMATION, MADTS
SOFTWARE DIAGNOSTIC PROGRAMS

7.1 GENERAL. The MADTS contains both PROM base firmware and disk base software. Upon boot, the MADTS performs a series of self-tests which are controlled by the PROM based MADTS. The first part of the self-test, tests all of the MADTS CPU general registers, data paths, and many instructions. If the test fails, the CPU will enter a wait state, which indicates a problem with the bus or the CPU card. If the test is successful, the MADTS will sound a bell tone and print out the following message:

SELFTEST [CPU RAM

Next, MADTS will perform a test of the RAM and Q-Bus signals. Note that the CPU mnemonic is output at the end of the CPU test, while all tests will output their respective mnemonic before test execution. If a bus error is detected during the RAM test, the system may crash. Otherwise, detection of an error will result in a scope loop or loop on error with bell tone. If the test is successful, MADTS will print:

REF

Refresh is the next test MADTS will perform. If during this test an error occurs the system will enter a WAIT state. If the test is successful, MADTS will print:

PAT

The Pattern test performs tests on memory locations. All of the RAM is tested from address 0 thru 157777, which is the first 28K words. If an error is detected during this test the system will enter a WAIT state. If the test is successful, MADTS will print:

ADR

ADR is a unique-address test which is performed on the first 28K words. If the test fails then the system will enter a WAIT state. If the test is successful, MADTS will print:

MMU

MMU is the Memory Management Unit Test. The existence of the MMU chip is verified. The processor will enter a WAIT state if an MMU is not present.

CPY

CPY is the Copy test testing the MRVII-C Control and Status Register (CSR) and the mapping windows. If an error is detected the system will either crash or it will loop on error with bell tone. If the test is successful, MADTS will copy the contents of the PROM into RAM, close the window and print:

XFR

XFR indicates that the MADTS has transferred the PROM instructions into RAM and that the self-test has finished successfully.

INT

INT is the Interrupt test. Two types of interrupts are tested while performing this test. The first type of interrupts tested is the Vectored Interrupts. These are software controlled interrupts and only after these are tested successfully does the test continue to test the Event Line Interrupts. If an error is detected during the Vector Interrupt test the system will attempt loop on error with bell tone. The same is true when testing the hardware controlled Event Line Interrupts. When both types of interrupts have been tested successfully, then MADTS prints:

XMM

XMM is the Extended Memory Test which tests and initializes extended memory. If an error is detected, the processor will enter a WAIT state.

Next MADTS will perform an automatic confidence check on certain critical MADTS LRUs and transfer to the disk based diagnostics.

Once MADTS is on the disk based system, MADTS will again perform an automatic confidence check on all of the MADTS LRUs. An example is shown in paragraph 7.2.

7.2 PREPARATION FOR TESTING. Test connections between the MADTS and the LRU being tested are described in the test procedure for that LRU.

CAUTION

Before installing or removing an LRU to the MADTS, set the power switch on the MADTS Electronics Drawer to OFF. This will minimize the possibility of damage to the MADTS or the LRU.

Prior to conducting a test ensure that the LRU under test is properly configured. After proper connections are made to the test LRU, set the POWER switch on the Electronics Drawer to ON. Then, the MADTS goes into a bootstrap diagnostics sequence which allows the disk drive(s) to spin up, and other checks to be made. The MADTS does a self-test and performs an automatic confidence check, which is a quick test of the MADTS LRUs. Before each test, the LRU mnemonic is printed. After the conclusion of each test, a test status indication of the LRU is printed. Included on the print out is a Rule which indicates the unit number of the device checked. An example is shown here.

```

KD          *
KT          *
AN          .....*****..
CI          ?
DL          .....
FP          .
IP          .
KB          *
KP          *
LA          *
LP          *
MP          *.....
MR          *
MS          *
MX          ????
RL          **??
TA          .
TK          .

```

The mnemonics and the LRU they represent are:

```

KD - Digital KDF11-AA Microcomputer
KT - Digital KTF11-AA Memory Management
AN - Alphanumeric OTF/Quad Cache
CI - CTS Interface
DL - TMI 8S
FP - Digital KEF11-AA Floating Point
IP - Peritek DMA-Q/HEX-L11 Diagnostic
KB - AFSS Position Keyboard
KP - Digital KPV11-B
LA - Digital LA34/LA100 IOT
LP - Printronix Line Printer
MP - Digital Memory Parity
MR - Digital MRV11-C PROM
MS - Digital MSV11-L RAM
MX - E-Systems Communications Multiplexer
RL - Digital RLV12/RL01/RL02
TA - Tandem-Ampex 9300 Disk Drive
TK - Tandem-Kennedy 9000 Tape Drive

```

The indicators to the right of each mnemonic have the following meaning:

- * - indicates proper response to automatic confidence check,
- ? - indicates questionable response to automatic confidence check, and
- . - indicates no response from the section or channel of the LRU checked.

Multiple indicators show the condition of each section or channel of the LRU checked, as some checks test only selected section of the test LRU. The indicators will reflect the condition and configuration of the MADTS. This will cause the responses to change as devices are connected or disconnected.

After the confidence check is complete, the MADTS prompt signal is printed, a colon (:). The MADTS then waits for a command.

There are four levels of commands to which the MADTS responds.

The first, or basic, level of command is indicated by no indentation of the printer. This level is primarily for selection of the device to be tested. The commands recognized at this level are listed below.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
D	Device Name	Selects device when followed by device mnemonic, and proceeds to the next second level, or prints a listing of mnemonics identification when no mnemonic is selected.
S	Set	Select or de-select options.
B	Boot	Boot MADTS.
H	Help	Prints list of commands and options for this level.

After the completion of every keyboard command input, the carriage return key must be pressed. This indicates that the command entered is to be executed. The carriage return key must be pressed after each and every input unless otherwise noted.

The second level of commands is indicated by indentation of the printer to the first 'tab' position. This level is primarily for the selection of the device program to be executed. In addition, options applicable to all programs of the given device may be selected. If a device is selected at level one which has only one device program, the monitor will automatically skip this level and proceed to the third level. The commands recognized at this level are listed below.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
P	Program	Selects program for execution and proceeds to third level.
S	Set	Selects options.
H	Help	Prints list of available commands, options, functions.
Escape	(Escape key)	Reverts to previous level.
B	Boot	Invoke device-specific bootstrap.

The third level of commands is indicated by the printer moving to the second 'tab' position. This level is primarily intended for initiation of the previously selected program. Additionally, program options may be selected, and individual functions of the program may be enabled or disabled. Commands recognized at this level are listed below.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
H	Help	Prints a list of available commands, options, and selectable functions.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
S	Set	Select options and select, or deselect functions.
X	Execute	Run the selected program.
I	Init Bus	Invoke Q-Bus Init.
Escape	(Escape Key)	Reverts to previous level.

In the second or third levels, the operator may revert to the previous command level by pressing the ESC key on the keyboard. The ESC key may also be used to terminate the printing out of a long error message or to abort the execution of functions which have been looping. If the ESC key is used during program execution, the program is suspended at the earliest possibility, and a fourth level is entered, indicated by the printer moving to a third 'tab' position. The commands recognized at this level are listed below.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
C	Continue	Continue execution of program from point of suspension (if was the result of pressing the "ESC"key).
R	Retry	Retry execution of the current function (If suspension was the result of an error report).
S	Set	Select options and select, or deselect functions.
H	Help	Print a list of available commands, options, and functions.

<u>COMMAND MNEMONIC</u>	<u>MEANING</u>	<u>ACTION</u>
Escape	(ESCAPE KEY)	Reverts to previous level.

When the 'Help' command is given, the options and functions available at that level are printed out, in addition to the commands. The functions differ for each LRU, but the options are standard. The options listed below are:

<u>NAME</u>	<u>MEANING</u>	<u>VALUE</u>	<u>EFFECT</u>
LE	Loop on Error	on/off	Continue executing stimulus/function causing error as long as error persists.
BE	Bell on Error	on/off	Issue bell tone whenever error is encountered.
AE	Abort on Error	on/off	Abort program execution upon error; else proceed to test next device unit using same program.
SE	Suspend on Error	on/off	Suspend function execution upon encountering error so that operator can issue commands or take corrective action.
PA	Pause on Request	on/off	If enabled, stimuli which include a pause will wait indefinitely until a KB input is received. Otherwise, the pause will be approximately 2 seconds. This option applies to the diagnostic programs for the AN, CI, IP, and MX devices.
RE	Registers on Error	on/off	Include CSR bank readout in the form of bit field composition with error report as applicable to certain programs.
DE	Dump on Error	on/off	Annotated dump on error-related data as applicable to certain programs.

<u>NAME</u>	<u>MEANING</u>	<u>VALUE</u>	<u>EFFECT</u>
CĒ	Continue on Error	on/off	If enabled, reporting of some errors are suppressed and operation continues. Where a significant error has occurred, operation aborts, reports are written, and the system reverts to level 3. This option is not supported by all diagnostic programs.
FT	Full Test	on/off	Execute certain functions in a special "exhaustive" mode.
PR	Progress Report	on/off	Issue stream of function mnemonics to console as they begin execution.
ER	Error Report	on/off	Issue error report to console when error encountered.
LP	Loop Program		Loop until escape the specified program.
LF*	Loop on Function	FUNC name	Loop until escape the specified function when the function is encountered in normal course.
SF*	Suspend on Function	FUNC name	Suspend program execution upon start of specified function so that operator may issue commands.
SU*	Starting Unit	Unit #	Unit number, starting at 0, of first device unit, or channel, to be tested. Automatically set to zero for single unit devices.
EU*	Ending Unit	Unit #	Unit number of last device unit, or channel, to be tested. Automatically set to zero for single unit devices.

There are two general formats for entering option selections. The first is as follows: (where [] indicates optional entries):

S +option mnemonic [-option mnemonic+....
 ..+option mnemonic] ENTER

The second type, indicated by * following the option name, is set by equating the name to the desired unit number or function mnemonic.

EXAMPLE: S SU=1+EU=4

The example sets the starting unit as number 1, and the ending unit as number 4. The tests selected at the program level will be run on units 1,2,3, and 4.

EXAMPLE: S LF=XXX+SF=YYY

This example will cause the monitor to loop on the XXX function and suspend on the YYY function when each is encountered in the course of program execution.

In setting options, take care to deselect conflicting options. In some cases, the order in which options are scanned prevent the desired action from occurring because the conflicting option has preempted the expected option. As is necessary for a complete test, the default setting of the options requires the operator to interact with the system. Under some conditions, it is necessary to test the unit for long periods to detect and to analyze intermittent failures or to ensure that repair is accomplished. The option settings allow the system to be set to run repetitively through most of the functions, issuing progress reports, aborting or not aborting on errors, and making full or abbreviated reports on errors as they occur. This flexibility requires that the operator is familiar with the effects of each option, and with the potential interactions of conflicting options. For instance, if both AE and LE are enabled when an error occurs, the LE takes precedence and the system will loop on error until the E scope key is typed, even though the operator may have wanted to input a command at the point of the error.

If an error is detected and reported during the course of a diagnostic, MADTS can respond in one of four ways. The possible responses and the necessary option settings are described below. Options not specified are left to operator preference.

1. Continuously retry the error until the Escape Key is typed.

Enabled: LE

No Effect: AE, SE, LP

NOTE

If an adequate loop is not produced, the enabling of LF for the current function may produce the desired results.

2. Suspend at level 4 of the monitor and wait for operator input.

Enabled: AE, SE

Disabled: LE

3. Abort the test and return to level 3 of the monitor.

Enabled: AE

Disabled: LE, SE

4. Abort the test and continue testing the remaining units (if any).

Disabled: LE, SE, AE

SECTION VIII
LRU TEST PROCEDURES
A/N OTF PROCESSOR ASSEMBLY

8.1 GENERAL. This section contains the test procedures for A/N OTF Processor assembly P/N 401-33676, as tested by the MADTS. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

8.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the A/N OTF:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostics Test Set (MADTS)	E-Systems P/N 401-37570-01
PROM	E-Systems P/N 316-3012-001

Tools other than standard shop tools are not required for test.

8.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the A/N OTF Processor schematic diagram, drawing no. 401-33665, and assembly drawing, drawing no. 401-33676. Refer to M1FC FSAS Equipment Instruction Book TI 6490.37 for these diagrams. Refer to M1FC FSAS System Instruction Book TI 6490.36 for the configuration specifications.

8.4 PREPARATION FOR TEST. To prepare the A/N OTF Processor for test, follow the instructions listed below.

1. Verify that one of PROM's listed in Table 8-2 is installed in socket U60 of A/N OTF Processor CCA (unit under test). If not, install PROM 316-3012-001 in socket U60, and remove it when test is complete.
2. Verify that System Power Switch is in ON position.
3. Set Electronics Chassis Power Switch to OFF.
4. Insert standard DEC quad extender board into slot A3-1 in card cage of Electronics Chassis. Observe correct key polarity so that extender board is oriented correctly with respect to its key.
5. Remove system Quad Cache CCA from slot A4-1. Insert system Quad Cache CCA into slot A4-2. Observe correct key polarity so that CCA is oriented correctly with respect to its key.

6. Insert A/N OTF Processor CCA (unit under test) into extender board. Observe correct key polarity so that CCA is oriented correctly with respect to its key.
7. Install P3 of ribbon cables W13, W14, W15, and W16 coming from Quad Cache CCA in slot A4-2 into J1, J2, J3, and J4 respectively, on A/N OTF Processor CCA under test.
8. Set switches on I/O CONTROL PANEL in accordance with Table 8-1.

Table 8-1. Initial Switch Settings

<u>SWITCH</u>	<u>POSITION</u>
1. KEYBOARD OUTPUT SELECT	X
2. SYNC SELECT	OTF PROCESSOR
3. SYSTEM ADDRESS BIM	X
4. SYSTEM ADDRESS CACHE	1-4
5. VIDEO SELECT	TEST CACHE 1
6. ELECTRONICS CHASSIS POWER	ON

X = Don't Care (Any Position)

8.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B..

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D AN (CR)

Printer response:

AN :

2. Input: P CNTL (CR)

Printer response:

ANCNTL:

3. Refer to Table 8-2. for correct operator input.

Table 8-2. Test Unit Number Set-Up

<u>PROM</u>	<u>Operator Input</u>
1. 316-3012-001	S SU=0+EU=3 (CR)
2. 316-3013-001	S SU=8+EU=11 (CR)
3. 316-3014-001	S SU=16+EU=19 (CR)
4. 316-3015-001	S SU=24+EU=27 (CR)
5. 316-3016-001	S SU=32+EU=35 (CR)

Printer response:

ANCNTL:

4. Input: X (CR)

Printer response:

X.
 00[CSR BUS UNT ADR BSL]
 01[CSR BUS UNT ADR BSL]
 02[CSR BUS UNT ADR BSL]
 03[CSR BUS UNT ADR BSL]

ANCNTL:

NOTE

The diagnostic program assumes M1FC hardware as the default. If a Model 1 OTF is detected, an appropriate message is output and the diagnostic will automatically reconfigure to correctly test the A/N OTF Processor.

5. The CNTL test has ended. Exit by pressing the ESC key.

Input: ESC-key

Printer response:

\$

AN :

6. Input: P DISP (CR)

Printer response:

ANDISP:

7. Input: X (CR)

Printer response:

X.

00[RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue

NOTE

The diagnostic program assumes M1FC hardware as the default. If a Model 1 OTF/Cache is detected, an appropriate message is output and the diagnostic will automatically reconfigure to correctly test the device.

Verify that the monitor display is the same as Figure 8-1.

9. Change the VIDEO SELECT switch to TEST CACHE positions 2, 3, and 4 and verify that the Figure 8-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 1.

Input: (CR)

Printer response:

ATD

Press RETURN to continue

10. Verify that the monitor display is the same as Figure 8-2.

Input: (CR)

Printer response:

PAT

Press RETURN to continue

= 40	8 = 70	P = 120	h = 150
! = 41	9 = 71	Q = 121	i = 151
" = 42	: = 72	R = 122	j = 152
# = 43	; = 73	S = 123	k = 153
\$ = 44	< = 74	T = 124	l = 154
% = 45	= = 75	U = 125	m = 155
& = 46	> = 76	V = 126	n = 156
' = 47	? = 77	W = 127	o = 157
(= 50	@ = 100	X = 130	p = 160
) = 51	A = 1-1	Y = 131	q = 161
* = 52	B = 102	Z = 132	r = 162
+ = 53	C = 103	[= 133	s = 163
, = 54	D = 104	/ = 134	t = 164
- = 55	E = 105] = 135	u = 165
. = 56	F = 106	^ = 136	v = 166
/ = 57	G = 107	_ = 137	w = 167
0 = 60	H = 110	` = 140	x = 170
1 = 61	I = 111	a = 141	y = 171
2 = 62	J = 112	b = 142	z = 172
3 = 63	K = 113	c = 143	← = 173
4 = 64	L = 114	d = 144	↑ = 174
5 = 65	M = 115	e = 145	→ = 175
6 = 66	N = 116	f = 146	↓ = 176
7 = 67	O = 117	g = 147	= 177

Figure 8-1. ASCII Test Pattern (ASC)

11. Verify that the monitor display is the same as Figure 8-3.
Set the VIDEO SELECT SWITCH to TEST CACHE 2.

Input: (CR)

Printer response:

```
]
01[ RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue
```

12. Verify that the monitor display is the same as Figure 8-1.

13. Change the VIDEO SELECT switch to TEST CACHE positions 1, 3 and 4 and verify that the Figure 8-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 2.

Input: (CR)

Printer response:

```
ATD
Press RETURN to continue
```

14. Verify that the monitor display is the same as Figure 8-2.

Input: (CR)

Printer response:

```
PAT
Press RETURN to continue
```

15. Verify that the monitor display is the same as Figure 8-3.
Set the VIDEO SELECT switch to TEST CACHE 3.

Input: (CR)

Printer response:

```
]
02 [ RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue
```

16. Verify that the monitor display is the same as Figure 8-1.

17. Change the VIDEO SELECT switch to TEST CACHE positions 1, 2 and 4 and verify that the Figure 8-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 3.

Input: (CR)

Printer response:

ATD
Press RETURN to continue

18. Verify that the monitor display is the same as Figure 8-2.

Input: (CR)

Printer response:

PAT
Press RETURN to continue

19. Verify that the monitor display is the same as Figure 8-3.
Set the VIDEO SELECT switch to TEST CACHE 4.

Input: (CR)

Printer response:

]
03 [RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue

20. Verify that the monitor display is the same as Figure 8-1.

21. Change the VIDEO SELECT switch to TEST CACHE positions 1, 2, and 3 and verify that the Figure 8-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 4.

Input: (CR)

Printer response:

ATD
Press RETURN to continue

22. Verify that the monitor display is the same as Figure 8-2.

Input: (CR)

Printer response:

PAT
Press RETURN to continue

23. Verify that the monitor display is the same as Figure 8-3.

Input: (CR)

Printer response:

]
ANDISP:

24. The A/N OTF Processor CCA diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.
25. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 8.7 and Table 8-3 or Table 9-3, OTF-Cache Error Messages depending on which function detected the error. These tables list the test functions, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the M1FC FSAS Equipment Instruction Book (TI 6490.37) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

NOTE

Disabling of the PA option will suppress the "Press RETURN to continue" prompt and instead delay 2 seconds before continuing.

NOTE

Enabling of the FT option will force a "board wide" test for the non-fill functions and more extensive verification during the fill functions. Test times are greatly extended, however.

8.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove all cables from A/N OTF Processor CCA under test.
4. Remove A/N OTF Processor CCA from extender board.
5. If another A/N OTF Processor CCA is to be tested, return to paragraph 8.4 and proceed.
6. Remove extender board from MADTS card cage.
7. Move System Quad Cache CCA from slot A4-2 to slot A4-1.

8.7 MADTS OTF PROCESSOR DIAGNOSTIC PROGRAM.

TYPE: A/N OTF #N
A CRT'S: POS 1-8
PART NUMBER: 401-33676

ID: A/N OTF PROCESSOR #N
B CRT'S: POS 9-16
CONFIGURE PER SPEC: 406-02165

8.7.1 Function Mnemonics. The following test function mnemonics are used by the OTF processor diagnostic program. Unless otherwise noted, functions are enabled by default for both the manual and automatic test modes.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. CSR	Ensures that the CSR can be accessed.
b. BUS	Ensures that the bus select bit can be set.
c. UNT	Ensures that unit numbers 1-8 can be written into the CSR unit select field.
d. ADR	Ensures that the proper cache unit is addressed when selected.
e. BSL	Tests the automatic bus deselect operation of the A/N OTF processor. This test requires two A/N OTF processors be connected by a ribbon cable. Disabled by default for both test modes.

8.7.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus will cause error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data are contained in Table 8-3. The address and contents of a CSR are normally given in the Bit Field Decomposition format, denoted by [BFD].

8.7.3 Error Output. Error codes and any associated data are output in the following form:

```
ERROR #xxxx      aaaaaa   bbbbbb   cccccc   dddddd
```

```
where:  xxxx   is the error number
        aaaaaa is the first output parameter
        bbbbbb is the second output parameter
        cccccc is the third output parameter
        dddddd is the fourth output parameter
```

The number of output parameters varies from 0 to 4 depending on the error. The error codes used by the A/N OTF Processor diagnostic program and their associated output parameters are given in Table 8-3.

This line demonstrates the CURSOR attribute
 This line demonstrates the BACKGROUND attribute
 This line demonstrates the REVERSE VIDEO attribute
 This line demonstrates the BLINKING attribute
 This line demonstrates the EMPHASIS attribute

```

ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01
BCDEFGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012
CDEFGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123
DEFGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01234
EFGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012345
FGHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456
GHIJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01234567
HJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012345678
IJKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:
KLMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]^`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?
  
```

Figure 8-2. Attribute Test Pattern (ATD)

NOTE:

1. The word CURSOR should have a cursor (underscore) that blinks at the rate of 1.25 Hz (0.8 seconds cycle time). Text lines 1, 6 and 11 should also have the cursor attribute.
2. The word BACKGROUND should be at half the normal intensity. Lines 2, 7 and 12 should also have the background attribute.
3. The words REVERSE VIDEO should be black-on-green. Lines 3, 8 and 13 should also have the reverse video attribute.
4. The word BLINKING should blink at the rate of 1.25 Hz (0.8 seconds cycle time). Lines 4, 9, and 14 should also have the blink attribute.
5. The word EMPHASIS should be "flickering" (intensity modulating) at the rate of 3 Hz. Lines 5, 10, and 15 should also have the emphasis attribute.

```

ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01
BCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012
CDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123
DEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01234
EFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012345
FGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456
GHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./01234567
HJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./012345678
IJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:
KLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?
PQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@
QRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@A
RSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@AB
STUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABC
TUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABCD
UVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABCDE
VWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABCDEF
WXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFG
XYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!~!"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGH

```

Figure 8-3. Pattern (PAT)

Table 8-3. A/N OTF Processor Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CSR	Read CSR	The OTF Processor CSR is read. If a bus timeout does not occur, the ready bit is tested to ensure that the OTF is not in a fill mode.	0	A bus timeout occurred while attempting to read the CSR.	CSR address
			2	The CSR ready bit is not set. The OTF and its associated cache memories are not usable.	CSR contents (BFD)
BUS	Enable Bus Control	The CSR is cleared. The bus control bit is set. If a bus timeout does not occur, the bus control bit is checked to ensure that it did get set.	4	A bus timeout occurred while attempting to write to the CSR.	CSR contents (BFD)
			6	The bus control bit in the CSR could not be set.	CSR contents (BFD)
UNT	Verify Unit Select	For unit numbers 1-8, the unit number is written to the unit select field of the CSR. The unit number is then read back and verified.	8	An unexpected unit number was read from the CSR unit select field.	CSR contents (BFD) Expected unit no.

Table 8-3. A/N OTF Processor Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ADR	Verify Unit Address	A unique value is written to the first word of each cache memory. Each value is then read back and verified. A bus timeout on a write operation indicates a nonexistent cache memory. Any non-existent units will be excluded from further testing within this function.	10	A unit addressing failure occurred. A value read from a cache unit is different from what was written to the unit.	CSR contents (BFD) Expected value Actual value
BSL	Deselect Ref. OTF	The reference (MADTS) OTF is selected. The test OTF is then selected. The seizure of the bus by the test OTF is verified by checking the CSR bus control bit of both OTFs.	12 14	Reference OTF does not respond. A bus timeout occurred while trying to access the resident OTF CSR. Unable to set the bus control bit in the CSR of the test OTF.	CSR address of reference OTF CSR contents of test OTF (BFD) Address of reference OTF CSR. Contents of reference OTF CSR

Table 8-3. A/N OTF Processor Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
BSL (con'd)			16	Reference OTF failed to release bus control when the bus was seized by the test OTF.	CSR contents of test OTF (BFD). Address of reference OTF CSR. Contents of reference OTF CSR.
	Deselect Test OTF	The reference (MADTS) OTF is selected. The seizure of the bus by the reference OTF is verified by checking the CSR bus control bit of both OTFs.	18	Reference OTF is unable to seize bus control.	CSR contents of test OTF (BFD). Address of reference OTF CSR. Contents of reference OTF CSR.
			20	Test OTF failed to release bus control when the bus was seized by the reference OTF.	CSR contents of test OTF (BFD). Address of reference OTF CSR. Contents of reference OTF CSR.

SECTION IX
LRU TEST PROCEDURES
QUAD CACHE ASSEMBLY
P/N 401-33692

9.1 GENERAL. - This section contains the test procedures for Quad Cache assembly P/N 401-33692, as tested by the MADTS. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

9.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Quad Cache:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostics Test Set (MADTS)	E-Systems P/N 401-37570-01
PROM	E-Systems P/N 316-3040-001

Tools other than standard shop tools are not required for test.

9.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the Quad Cache schematic diagram, drawing no. 401-33690, and assembly drawing, drawing no. 401-33692. Refer to M1FC FSAS Equipment Instruction Book TI 6490.37 for these diagrams. Refer to M1FC FSAS System Instruction Book TI 6490.36 for the configuration specifications.

9.4 PREPARATION FOR TEST. To prepare the Quad Cache for test, follow the instructions listed below.

1. Verify that one of PROM's listed in Table 9-2 is installed in socket U5 of QUAD CACHE CCA (unit under test). If not, install P/N 316-3040-001 in socket U5, and remove it when test is complete.
2. Verify that System power switch is in ON position.
3. Set Electronics Chassis power switch to OFF.
4. Insert standard DEC quad extender board into slot A4-2 in card cage of electronics chassis. Observe correct key polarity so that extender board is oriented correctly with respect to its key.
5. Insert Quad Cache CCA (unit under test) into extender board. Observe correct key polarity so that CCA is oriented correctly with respect to its key.

6. Install P3 of ribbon cables W13, W14, W15, W16 coming from QUAD CACHE CCA in slot A4-1 into J1, J2, J3, and J4 respectively, on Quad Cache CCA under test.
7. Set switches on I/O CONTROL PANEL in accordance with Table 9-1.

Table 9-1. Initial Switch Settings

<u>SWITCH</u>	<u>POSITION</u>
1. KEYBOARD	X
2. SYNC SELECT	OTF [PROCESSOR
3. SYSTEM ADDRESS BIM	X
4. SYSTEM ADDRESS CACHE	(See Table 9-2)
5. VIDEO SELECT	TEST CACHE 1
6. ELECTRONICS CHASSIS POWER	ON

X = Don't Care (Any Position)

9.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Derot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D AN (CR)

Printer response:

AN :

2. Input: P DISP (CR)

Printer response:

ANDISP:

3. Refer to Table 9-2 for correct operator input and switch settings.

Table 9-2. Test Unit Number Set-Up

<u>PROM</u>	<u>Switch Setting</u> <u>SYSTEM ADDRESS CACHE</u>	<u>Operator Input</u>
1. 316-3040-001	5-8	S SU=40+EU=43 (CR)
2. 316-3041-001	1-4	S SU=44+EU=47 (CR)

Printer response:

ANDISP:

4. Input: X (CR)

Printer response:

X
40[RWT CEL UAD CCC CUA CBF HBF WDF LNF VRF ASC
Press RETURN to continue

NOTE

The diagnostic program assumes M1FC hardware as the default. If a Model 1 OTF/cache is detected, an appropriate message is output and the diagnostic will automatically reconfigure to correctly test the device.

5. Verify that the monitor display is the same as Figure 9-1.
6. Change the VIDEO SELECT switch to TEST CACHE positions 2, 3, and 4 and verify that the Figure 9-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 1.

= 40	8 = 70	P = 120	h = 150
! = 41	9 = 71	Q = 121	i = 151
" = 42	: = 72	R = 122	j = 152
# = 43	: = 73	S = 123	k = 153
\$ = 44	< = 74	T = 124	l = 154
% = 45	= = 75	U = 125	m = 155
& = 46	> = 76	V = 126	n = 126
' = 47	? = 77	W = 127	o = 157
(= 50	@ = 100	X = 130	p = 160
) = 51	A = 1-1	Y = 131	q = 161
* = 52	B = 102	Z = 132	r = 162
+ = 53	C = 103] = 133	s = 163
, = 54	D = 104	/ = 134	t = 164
- = 55	E = 105] = 135	u = 165
. = 56	F = 106	^ = 136	v = 166
/ = 57	G = 107	= = 137	w = 167
0 = 60	H = 110	~ = 140	x = 170
1 = 61	I = 111	a = 141	y = 171
2 = 62	J = 112	b = 142	z = 172
3 = 63	K = 113	c = 143	← = 173
4 = 64	L = 114	d = 144	↑ = 174
5 = 65	M = 115	e = 145	→ = 175
6 = 66	N = 116	f = 146	↓ = 176
7 = 67	O = 117	g = 147	= 177

Figure 9-1. ASCII Test Pattern (ASC)

7. Input: (CR)

Printer response:

ATD
Press RETURN to continue

8. Verify that the monitor display is the same as Figure 9-2.

9. Input: (CR)

Printer response:

PAT
Press RETURN to continue

10. Verify that the monitor display is the same as Figure 9-3. Set the VIDEO SELECT SWITCH to TEST CACHE 2.

11. Input: (CR)

Printer response:

]
41[RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue

12. Verify that the monitor display is the same as Figure 9-1.

13. Change the VIDEO SELECT switch to TEST CACHE positions 1, 3 and 4 and verify that the Figure 9-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 2.

14. Input: (CR)

Printer response:

ATD
Press RETURN to continue

15. Verify that the monitor display is the same as Figure 9-2.

16. Input: (CR)

Printer response:

PAT
Press RETURN to continue

17. Verify that the monitor display is the same as Figure 9-3. Set the VIDEO SELECT switch to TEST CACHE 3.

18. Input: (CR)

Printer response:

```
]
42[ RWT CEL UAD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue
```

19. Verify that the monitor display is the same as Figure 9-1.

20. Change the VIDEO SELECT switch to TEST CACHE position 1, 2, and 4 and verify that the Figure 9-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 3.

21. Input: (CR)

Printer response:

```
ATD
Press RETURN to continue
```

22. Verify that the monitor display is the same as Figure 9-2.

23. Input: (CR)

Printer response:

```
PAT
Press RETURN to continue
```

24. Verify that the monitor display is the same as Figure 9-3. Set the VIDEO SELECT switch to TEST CACHE 4.

25. Input: (CR)

Printer response:

```
]
43 [ RWT CEL CUD CCC CUA LBF HBF WDF LNF VRF ASC
Press RETURN to continue
```

26. Verify that the monitor display is the same as Figure 9-1.

27. Change the VIDEO SELECT switch to TEST CACHE positions 1, 2, and 3 and verify that the Figure 9-1 pattern does NOT appear on the monitor display. Set the VIDEO SELECT switch to TEST CACHE position 4.

28. Input: (CR)

Printer response:

```
ATD
Press RETURN to continue
```

29. Verify that the monitor display is the same as Figure 9-2.

30. Input: (CR)

Printer response:

PAT

Press RETURN to continue

31. Verify that the monitor display is the same as Figure 9-3.

32. Input: (CR)

Printer response:

]

ANDISP:

33. The Quad Cache CCA diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.

34. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 9.7 and Table 9-3, Quad Cache Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the M1FC FSAS Equipment Instruction Book (TI 6490.37) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

NOTE

Disabling of the PA option will suppress the "Press RETURN to continue" prompt and instead delay 2 seconds before continuing.

NOTE

Enabling of the FT option will force a "board wide" test for the non-fill functions and more extensive verification during the fill functions. Test times are greatly extended, however.

9.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis POWER switch to OFF position.

3. Remove all cables from Quad Cache CCA under test.
4. Remove Quad Cache CCA from extender board.
5. If another Quad Cache CCA is to be tested, return to paragraph 9-4 and proceed.
6. Remove extender board from MADTS card cage.

9.7 MADTS A/N OTF CACHE MEMORY DIAGNOSTIC PROGRAM.

TYPE: CACHE #N	ID: A/N CACHE MEMORY #N
A CRT'S: POS 1-16	PROGRAM PROM: 316-3040-001 (U5) - 316-3041-001 (U5)
PART NUMBER: 401-33692	CONFIGURE PER SPEC: 406-02166

9.7.1 Function Mnemonics

The following test function mnemonics are used by the alphanumeric cache memory diagnostic program. Unless otherwise noted, functions are enabled by default for the manual test mode and are disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. RWT	Ensures that a cache memory can be read from and written to. Enabled during the automatic test mode.
b. CEL	Exercises all noncontrol bits in each word (cell) of the cache memory.
c. UAD	Performs a unique address test on each word of the cache memory.
d. CCC	Exercises all noncontrol bits in each word of the cache memory with color enabled.
e. CUA	Performs a unique address test on each word of the cache memory with color enabled.
f. LBF	Performs a low byte fill test of cache memory using a replicating bit pattern (1, 3, 7, etc.) for the 7 character bits.
g. HBF	Performs a high byte fill test of cache memory using a replicating bit (1, 3, 7,) for the S attribute bits.
h. WDF	Performs a full word fill test of cache memory using values from 176 to 0.

- i. LNF Performs a word fill test of each 80 column line of cache memory using values from 176 to 0.
- j. VRF Performs a varying range fill test within each line.
- k. PAT Writes a rolling pattern display into cache memory.
- l. ATD Writes a video attribute display pattern into cache memory.
- m. COL Writes a color attribute display pattern into cache memory. This function is included only with systems that include a color display monitor.
- n. ASC Writes an ASCII character display into cache memory.
- o. DIA Continuously writes a specified character code to each word of cache memory for diagnostic purposes. Disabled by default for both test modes.

9.7.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data are contained in Table 9-3. The address and contents of a CSR is normally given in the BFD format.

9.7.3 Error Output. Error codes and any associated data are output in the form:

ERROR #xxxx aaaaaa bbbbbb cccccc ddddd

where: xxxx is the error number
 aaaaaa is the first output parameter
 bbbbbb is the second output parameter
 cccccc is the third output parameter
 ddddd is the fourth output parameter

The number of output parameters varies from 0 to 4 depending on the error. Additional error data can be given in an annotated dump format as follows:

ADDR	EXPCTD	ACTUAL
163636	050141	050140
163646	050141	050140
163656	050141	050140
163666	050141	050140
163676	050141	050140

Up to 10 lines can be output

The ADDR column base address will either be 000000 or 160000 depending on the hardware under test. When a Model 1 OTF/Cache is under test, addressing begins at 160000. M1FC OTF/Cache hardware is indicated by a base address of 000000, although it has an actual starting address of 400000.

The error codes used by the alphanumeric cache memory diagnostic program and their associated output parameters are given in Table 9-3.

This line demonstrates the CURSOR attribute
 This line demonstrates the BACKGROUND attribute
 This line demonstrates the REVERSE VIDEO attribute
 This line demonstrates the BLINKING attribute
 This line demonstrates the EMPHASIS attribute

```

ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./01
BCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./012
CDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123
DEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./01234
EFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./012345
FGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456
GHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./01234567
HIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./012345678
IJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:
JKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@! "$%&'()*+,-./0123456789:;<=>?
  
```

Figure 9-2. Attribute Test Pattern (ATD)

NOTE:

1. The word CURSOR should have a cursor (underscore) that blinks at the rate of 1.25 Hz (0.8 seconds cycle time). Text lines 1, 6 and 11 should also have the cursor attribute.
2. The word BACKGROUND should be at half the normal intensity. Liners 2, 7 and 12 should also have the background attribute.
3. The words REVERSE VIDEO should be black-on-green. Lines 3, 8 and 13 should also have the reverse video attribute.
4. The word BLINKING should blink at the rate of 1.25 Hz (0.8 seconds cycle time). Lines 4, 9, and 14 should also have the blink attribute.
5. The word EMPHASIS should be "flickering" (intensity modulating) at the rate of 3 Hz. Lines 5, 10, and 15 should also have the emphasis attribute.

```

ABCDEFGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./01
BCDEFGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012
CDEFGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123
DEFGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./01234
EFGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012345
FGHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456
GHIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./01234567
HIJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012345678
IJKLMNPOQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:
KLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?
PQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@
QRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@A
RSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@AB
STUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABC
TUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABCD
UVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABCDE
VWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABCDEF
WXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABCDEFG
XYZ[\]^_`abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?@ABCDEFGH

```

Figure 9-3. Pattern (PAT)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
RWT	Read Cache	The first cache word is read.	2	A bus timeout occurred while attempting to read a cache location.	Address causing timeout
	Write and Verify	A zero is written to the first cache word. If a bus timeout did not occur, the word is read and verified.	0	A bus timeout occurred while attempting to write to a cache location.	Address causing timeout CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Expected value actual value CSR contents (BFD)
CEL	Exercise all memory cells	Cache memory is cleared. If a bus timeout occurred it is reported. For each word of cache memory, the values 000000, 057577, 005052, and 052525 are each written, read block and verified. Errors are not reported until the stimulus has completed. Error information associated with the first 10 errors (or less) is retained.	0	A bus timeout occurred while attempting to write to a cache location.	Address causing timeout CSR contents (BFD)
			16	One or more values read from cache are different from what was previously written.	Annotated dump consisting of: address of error expected value actual value Total error count CSR contents (BFD)

10 max.

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
UAD	Unique Address	Cache memory is cleared. If a bus timeout error occurred, the error is reported. The first word of the cache is checked to ensure it is clear. A value of 057577 is written to the location. The procedure is repeated for each successive memory location. Error information associated with the first 10 (or less) errors is retained. Any bus timeout errors are reported immediately since further test results will no longer be valid.	0	A bus timeout occurred while attempting to write to a cache location.	CSR contents (BFD)
			2	A bus timeout occurred while attempting to read a cache location.	CSR contents (BFD)
			16	One or more values read from cache are different from what was previously written.	Annotated dump consisting of: Address of error Expected value 10 max. Actual value Total error count CSR contents (BFD)
CCC	Exercise all memory cells	Cache memory is cleared. If a bus timeout error occurred, the error is reported. For each word of cache memory, the values 020000, 077577, 025052, and 072525 are each written, read back, and verified. Errors are not reported until the stimulus has completed.	0	A bus timeout occurred while attempting to write to a cache location.	Address causing timeout CSR contents (BFD)
			16	One or more values read from cache are different from what was previously written.	Annotated dump consisting of: Address of error Expected value 10 max. Actual Value Total error count CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		Error information associated with the first 10 errors (or less) is retained.			
CUA	Unique Address	Cache memory is cleared. If a bus timeout error occurred, the error is reported. The first word of the cache memory is checked to ensure that it is clear (except the color control bit). A value of 077577 is written to the location. The procedure is repeated for each successive memory location. Error information associated with the first 10 errors (or less) is retained.	0	A bus timeout occurred while attempting to write to a cache location.	CSR contents (BFD)
			2	A bus timeout occurred while attempting to write to a cache location.	CSR contents (BFD)
		All	16	One or more values read from cache are different from what was previously written.	Annotated dump consisting of: Address of error Expected value 10 max. Actual value Total error count

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		Error information associated with the first 10 errors (or less) is retained.			
CUA	Unique Address	Cache memory is cleared. If a bus timeout error occurred, the error is reported. The first word of the cache memory is checked to ensure that it is clear (except the color control bit). A value of 077577 is written to the location. The procedure is repeated for each successive memory location. Error information associated with the first 10 errors (or less) is retained. All bus timeout errors are reported immediately since further tests results will no longer be valid.	0	A bus timeout occurred while attempting to write to a cache location.	CSR contents (BFD)
			2	A bus timeout occurred while attempting to write to a cache location.	CSR contents (BFD)
			16	One or more values read from cache are different from what was previously written.	Annotated dump consisting of: Address of error Expected value 10 max. Actual value Total error count CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LBF	Low Byte Fill	Cache memory is initialized with a value of 17400 in each location. A replicating bit pattern (1,3,7, etc.) is used to test the low byte fill of the entire cache memory.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Address of the word filled Expected value (0500) Actual Value CSR contents (BFD)
			8	A screen fill operation did not complete within the allotted time.	CSR contents (BFD) Address of the word filled Value following filled word CSR contents (BFD)
HBF	High Byte Fill	Cache memory is initialized with a value of 176 in each location. A replicating bit pattern (1,3,7,17,37) is used to test the high byte fill of the entire cache memory.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Address the word filled Expected value Actual value CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			8	A screen fill operation did not complete within the allotted time.	CSR contents (BFD)
WDF	Word Fill	Cache memory is initialized with a value of 177 in each location. For all values from 176 to 0, a full word screen fill is performed and verified.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Address of the word filled Expected value Actual Value CSR contents (BFD)
			8	A screen fill operation did not complete within the allotted time.	CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LNF	Line Fill	Cache memory is initialized with a value of 177 in each location. For all values from 176 to 0, a full word line fill (80 columns) is performed and verified. All 24 display lines are tested.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Address of the word filled Expected value Actual value CSR contents (BFD)
			8	A screen fill operation did not complete within the allotted time.	CSR contents (BFD)
VRF	Variable Range Fill	Each location of cache memory is initialized with its unique address. For each displayable line, an increasing range word fill is performed. A blank is filled from column 1 to column 2, 1 to 3, 1 to 4, etc. After each operation, the fill is verified and the range re-initialized.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
			4	A value read from cache is different from what was previously written to the location.	Address of the word filled Expected value Actual value CSR contents (BFD)
			8	A screen fill operation did not complete within the allotted time.	CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			10	A fill operation overran the specified fill range.	Address of the word Expected value Actual value Line number CSR contents (BFD)
PAT	Output rolling pattern	Write a rolling pattern for the purpose of visual screen verification.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
ATD	Output attribute display	Write a video attribute display for the purpose of visual screen verification.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)
ASC	Output ASCII Code Display	Write an ASCII character display for the purpose of visual screen verification.	0	A bus timeout occurred while attempting to write to a cache location.	Address of the word CSR contents (BFD)

Table 9-3. A/N OTF-Cache Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DIA	Character Write	Continuously writes a specified character code to each word of cache memory for diagnostic purposes. The operator is prompted to enter a character that is then continuously written to entire cache memory. The character that is input is written to all cache memory locations until ESCAPE key is typed, causing suspension at the highest indentation level. This test is provided as an aid in diagnosing the cache video output circuitry and is disabled by default.	none		

SECTION X
LRU TEST PROCEDURES
MULTIPLEXER ASSEMBLY

10.1 GENERAL. This section contains the test procedures for Multiplexer assembly P/N 401-36993, as tested by the MADTS. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

10.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Multiplexer:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostics Test Set (MADTS)	E-Systems P/N 401-37570-01
Control Status Register (CSR) Address Jumper	401-37124-01
DEC Quad Extender Board	W987-00
32 Circuit Patch Cord (2 each)	Dynatech DPC-32-Y
Berg Jumper (2 each)	76264-101

Tools other than standard shop tools are not required for test.

10.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the Multiplexer schematic diagram, drawing no. 401-36992, and assembly drawing, drawing no. 401-36993. Refer to M1FC FSAS Equipment Instruction Book TI 6490.37 for these diagrams. Refer to M1FC FSAS System Instruction Book TI 6490.36 for the configuration specifications.

10.4 PREPARATION FOR TEST. To prepare the Multiplexer for test, follow the instructions listed below.

1. Verify that System power switch is in ON position.
2. Set Electronic Chassis power switch to OFF.
3. Disconnect ribbon cable P/N 401-37759-01, W9, P-2 from J-2 on MADTS system Multiplexer CCA and ribbon cable P/N 401-37759-01, W10, P-2 from J-1 on MADTS system Multiplexer CCA.
4. Remove MADTS system Multiplexer CCA from slot A2-2 in MADTS Card Cage.
5. Insert standard DEC quad board extender into slot A2-2 in Card Cage of Electronics Chassis so that board extender is oriented correctly with respect to its key.

6. Insert Multiplexer CCA (unit under test) into board extender so that Multiplexer CCA is oriented correctly with respect to its key.
7. Connect ribbon cable P/N 401-37759-01, W9, P-2 to J-2 on Multiplexer CCA. Connect ribbon cable P/N 401-37759-01, W10, P-2 to J-1 on Multiplexer CCA.
8. Verify that one of following CSR address jumpers is installed in Multiplexer CCA socket U93.

401-37124-01 - Option Plug Assembly-U93 Address
Configuration-Mux

401-37124-02 - Option Plug Assembly-U93 Address
Configuration-Mux

If there is no jumper, install jumper part number 401-37124-01 in Multiplexer CCA socket U93, and remove it when test is complete.

9. Set Modem E-208A (in Card Cage RM-8E, Slot 1) switches to following positions:

a. ST/STRO switch to NORM

b. AL/DL switch to NORM

10-5. TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MX (CR)

Printer response:

MXDIAG:

2. Refer to Table 10-1 for correct operator input.

Table 10-1. Test Unit Number Set-Up

<u>Jumper In Socket U93</u>	<u>Operator Input</u>	
1. 401-37124-01	S EU=3	(CR)
2. 401-37124-02	S SU=4+EU=7	(CR)

Printer response:

MXDIAG:

NOTE

The first two digit number represented in the printer response in step 3 thru step 9 is related to the jumper located in U93. The two digit number shown is for jumper 401-37124-01. With jumper 401-37124-02 in U93 the two digit numbers are as follows:

Step 3 04, Step 5 05, Step 7 06, and Step 9 07.

3. Input: X (CR)

Printer response:

X.
00[CSR
CP Unit Number is 00

INT HDL TRN TRE ADR DLY
Press RETURN to Continue

NOTE

The CP unit number is a two digit number that corresponds to the configuration used.

NOTE

The ADR function is applicable to M1FC boards only. If a Model 1 board is under test, ADR should be disabled (S-ADR).

4. Connect digital patch panel cable P/N DPC-32-Y from Digital Patch Panel position RM-8E SLOT 1 to Digital Patch Panel position MUX CHAN 1.

5. Input: (CR)

Printer response:

```

]
01 [ CSR
    CP unit number is 00
    INT HDL TRN TRE ADR DLY
    Press RETURN to continue

```

6. Disconnect digital patch panel cable P/N DPC-32-Y from Digital Patch Panel position MUX CHAN 1, and reconnect the digital patch panel cable to Digital Patch Panel position MUX CHAN 2 are now connected. Connect a second digital patch panel cable P/N DPC-32-Y from Digital Patch Panel position RM-12E SLOT 1 to Digital Patch Panel position MONITOR. (use DPC-24-3 for this)

7. Input: (CR)

Printer response:

```

]
02 [ CSR
    CP Unit Number is 00

    INT HDL TRN TRE ADR DLY
    Press RETURN to continue

```

8. Disconnect digital patch panel cable P/N DPC-32-Y from Digital Patch Panel position MUX CHAN 2, and reconnect the digital patch panel cable to Digital Patch Panel position MUX CHAN 3. Digital Patch Panel positions RM-8E SLOT 1 and MUX CHAN 3 are now connected.

9. Input: (CR)

Printer response:

```

]
03 [ CSR
    CP Unit Number is 00

    INT HDL TRN TRE ADR DLY
    Press RETURN to continue

```

10. Input: (CR)

Printer response:

]
MXDIAG

11. The Multiplexer CCA diagnostic test is complete.
If no errors were reported by MADTS, the CCA is good.
12. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 10.7 and to Table 10.2, Multiplexer Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the M1FC FSAS Equipment Instruction Book (TI 6490.37) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

10.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronic Chassis POWER Switch to OFF position.
3. Disconnect ribbon cable P/N 401-37559-01, W9, P-2 from J-2 on the Multiplexer CCA under test and ribbon cable P/N 401-37559-02, W10, P-2 from J-1 on Multiplexer CCA under test.
4. Remove Multiplexer CCA (unit under test) board extender.
5. If part number 401-37124-01 was installed in socket U93 by operator at beginning of this test, remove it.
6. Remove jumpers from E2 and E3 on Multiplexer CCA under test.
7. Remove all Digital Patch Panel cables, P/N DPC-32-Y
8. If additional Multiplexer CCA's are to be tested return to paragraph 10-4, step 6 and repeat test with next Multiplexer CCA. Otherwise, continue Power Down Sequence.
9. Remove board extender from card cage.
10. Replace MADTS system Multiplexer CCA into slot A2-2 in MADTS Card Cage.

11. Connect ribbon cable P/N 401-37759-01, W9, P-2 to J-2 on MADTS system Multiplexer CCA, and connect ribbon cable P/N 401-37759-01, W10, P-2 to J-1 on MADTS system Multiplexer CCA.

10.7 MADTS E-SYSTEMS MULTIPLEXER DIAGNOSTIC PROGRAM.

TYPE: MUX #1
PART NUMBER: 401-36993

I.D.: MULTIPLEXER #1
CONFIGURE PER SPEC: 406-02332

10.7.1 Function Mnemonics. The test function mnemonics used by the Multiplexer diagnostic program are given below. Unless otherwise noted, functions are enabled by default for both the manual test mode and the automatic test mode.

10.7.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 10-2. The address and contents of a CSR are normally given in the Bit Field Decomposition format, denoted by [BFD].

10.7.3 Error Output.

Error codes and any associated data are output in the form:

```
ERROR #xxxx      aaaaaa      bbbbbb      ccccc      dddddd
```

where:

```
xxxx    is the error number
aaaaaa  is the first output parameter
bbbbbb  is the second output parameter
cccccc  is the third output parameter
ddddd   is the fourth output parameter
```

The number of output parameters varies from zero to four depending on the error. Additional error data may be given in an annotated dump format as follows:

TRANSMIT BUFFER DUMP

```
TRANSMIT BUFFER DUMP
000001 001004 004020 020100 100377 000301 000310 000320
```

RECEIVE BUFFER DUMP

RECEIVE	BUFFER	DATA	DATA	DATA	DATA	DATA	DATA
000000	001004	004020	020100	100376	000007	000007	000007

The error codes used by the E-Systems Multiplexer diagnostic program and their associated output parameters are given in Table 10-2.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. CSR	Ensures that the MUX CSR can be read from and written to.
b. INT	Ensures that the MUX can be initialized properly. This function cannot be disabled.
c. LPB	Ensures that the MUX can be put into the on-board loopback mode. Disabled by default for the manual test mode.
d. HDL	Ensures that the selected channel can be put into the HDLC mode.
e. TRN	Tests the transmit and receive functions of the MUX using nonextended memory.
f. TRE	Tests the transmit and receive functions of the MUX using extended memory.
g. ADR	Tests the address search function of the MUX.
h. RLB	Ensures that the MUX can be taken out of on-board loopback mode. Disabled by default for the manual test mode.
i. PRI	Ensures that the selected channel can be put into the printer mode.
j. TPR	Tests the printer mode at selected channel.
k. DLY	Allows execution to be delayed until a character is typed. Disabled for the automatic test phase.

Table 10-2. MUX Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CSR	Read CSR	The MUX Control Status Register is read.	0	A bus timeout occurred while trying to read the MUX is not usable.	-
	Write to CSR	An Octal 60 is written to the CSR.	2	A bus timeout occurred while attempting to write the CSR.	CSR contents (BFD)
INT	Initialize MUX	The MUX is reset. A time interval of 2/60 of a second is allowed for the CSR Done bit to be set. The vector base address and the control/status segment base address is sent to the MUX via the CSR. Again, a 2/60 of a second time interval is allowed for the CSR Done bit to be set. All interrupts are then enabled.	4	The Done bit in the CSR was not set with in 2/60 of a second. The MUX is not usable.	CSR contents (BFD)

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LPB	Enable Loop-back	MUX on-board loopback is enabled. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loop-back status is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			10	An incorrect loop-back status was returned by the MUX after being put in the loopback mode.	Channel number under test
HDL	Enable HDLC Mode	The mode byte in the Channel Control Segment is set to indicate HDLC. The transmit service required byte is set and the CSR is strobed. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The channel mode is checked via the channel status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test The interrupt vector received
			12	An incorrect channel mode value was returned by the MUX.	Channel number under test Expected channel mode value (3) Channel mode value returned by the MUX

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
TRN	Transmit	A transmit operation is initiated with the transmit data and the receive buffer in non-extended memory. A time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector is then verified. A channel receive request is then made. A time interval of 5 seconds is also allowed for a receive interrupt to be generated by the MUX. The interrupt vector is then verified. The channel status segment is accessed to check for a transmit or receive error. The data received is then compared with the data transmitted.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Vector address received
			20	A transmit error occurred.	Channel number under test First three words of the channel status segment
			14	An expected receive interrupt was not received within the allotted time.	Channel number under test
			16	The receive interrupt was the wrong interrupt.	Channel number under test Interrupt vector received

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			22	A receive error occurred.	Channel number under test 5th thru 7th words of channel status segment
			18	Data received does not match the data transmitted.	64 words of transmit buffer 64 words of receive buffer Channel number under test
TRE	Transmit	A transmit operation is initiated with the transmit data and the receive buffer in extended memory a time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector then is verified. A channel request is made, and a time interval of 5 seconds is allowed for a receive interrupt to be generated by the MUX. The channel status segment is accessed to check	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			20	A transmit error occurred.	Channel number under test First three words of channel status segment

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		for a transmit or receive error. The data received is then compared with the data transmitted.			
			14	An expected receive interrupt was not received within the allotted time.	Channel number under test
			16	The receive interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received.
			22	A receive error occurred.	Channel number under test 5th thru 7th words of channel status segment
			18	Data received does not match the data transmitted.	64 words of transmit buffer 64 words of receive buffer Channel number under test

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ADR	ADR1	MUX address search is enabled. An invalid header address is transmitted. No receive interrupt should occur and no message should be received.	24	Message not filtered while in address search mode.	Channel No. Message header address
	ADR2	MUX address search is enabled. A valid header address is transmitted. The data is received and verified.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			20	A transmit error occurred.	Channel number under test First three words of channel status segment
			26	Data transfer error while in address search mode.	64 words of transmit buffer 64 words of receive buffer Channel number under test

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
RLB	Disable Loop-back	MUX on-board loopback is disabled. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loopback is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			10	An incorrect loopback status was returned by the MUX after loopback mode being removed.	Channel number under test
PRI	Enable printer mode	The selected channel is put into printer mode. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loopback status is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			12	An incorrect channel mode value was returned by the MUX.	Channel number under test The expected channel mode value (1) the channel mode value returned by the MUX

Table 10-2. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
TPR	Test printer mode	A transmit operation is initiated with the transmit data and the channel already in the printer mode. A time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector then is verified. The channel Status Segment is accessed to check for a transmit error.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test vector address received
			20	A transmit error occurred.	Channel number under test First three words of the channel status segment
DLY	Delay execution	A message is output to the console directing the operator to type a character when execution is to be continued. Execution of the diagnostic with resume when a character is entered.	none		

SECTION XI
LRU TEST PROCEDURES
CODED TIME SOURCE INTERFACE
CIRCUIT CARD ASSEMBLY

11.1 GENERAL. This section contains the test procedures for Coded Time Source Interface (CTSI) CCA P/N 401-36972, as tested by the MADTS. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

11.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the CTSI CCA:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostics Test Set (MADTS)	E-Systems P/N 401-37570-01
CTS Interface	E-Systems P/N 401-37207
Dual Extender Board	DEC P/N W984-00
MADTS Test Cable	E-Systems P/N 401-37876
MADTS Test Cable	E-Systems P/N 401-37849
MADTS Test Cable	E-Systems P/N 401-37126-07

Tools other than standard shop tools are not required for test.

11.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the Coded Time Source Interface schematic diagram, drawing no. 401-37221, and assembly drawing, drawing no. 401-37207. Refer to MIFC FSAS Equipment Instruction Book (TI 6490.37) for these diagrams.

11.4 PREPARATION FOR TEST. To prepare the CTSI CCA for test, follow the instructions listed below.

1. Verify that System power switch is in ON position.
2. Set Electronics Chassis Power switch to OFF.
3. Insert Coded Time Source Interface Circuit Board into Test Unit Coded Time Source Chassis.
4. Remove DRV11-J from slot A1-L4 in Electronics Chassis card cage.
5. Insert standard DEC dual extender board into slot A1-L4 in card cage of Electronics Chassis. Observe correct key polarity so that extender board is oriented correctly with respect to its key.

6. Insert DRV11-J into board extender. Observe correct key polarity so that DRV11-J is oriented correctly with respect to its key.
7. Connect cable P/N 401-37876-01, P1 to J3 on CTSI, and P2 to DRV11-J, J2. Connect cable P/N 401-37849-01, P2 to CTS J2, P3 to CTS TEST, and P1 to DRV11-J J1. Connect cable P/N 401-37126-07, P1 to CTS J1, and P2 to Channel 2 on MADTS TMI 8S Ports.

Before continuing, check S1 and S2 on PC Board inside of CTSI

S2

SWITCH	POSITION	FUNCTION
2	ON	ODD PARITY
3	ON	7 DATA BITS
4	OFF	
5	OFF	2 STOP BITS
6	ON	PARITY ENABLE
1	OFF	
7	OFF	
8	OFF	

S1

SWITCH	POSITION	FUNCTION
1	OFF	
2	ON	1CLK/2CLK
3	OFF	
8	ON	RTS CTS

S1

SWITCH	BAUD RATE
4 ON	2400

8. Set CTS AC Power Switch to ON position.

9. Set Electronics Chassis Power Switch to ON position.

11.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
                 KD      *
                 KT      *
                 KP      *
                 MP      *.....
                 MR      .....*...
                 MS      **.....
                 RL      *???....

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>*SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
                 KD      *
                 KT      *
                 AN      .....????****
                 CI      .
                 DL      .....*****
                 FP      *
                 IP      *..
                 KB      *
                 KP      *
                 LA      *
                 LP      *
                 MP      *.....
                 MR      .....*...
                 MS      **.....
                 MX      ****....
                 RL      *???....
                 TA      .
                 TK      .

                 0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D CI (CR)

Printer response:

CI :

2. Input: P PRL (CR)

Printer response:

CIPRL:

3. Input: X (CR)

Printer response:

X.
00[BIN LTX LAX LBX ABX]

CIPRL:

4. The PRL test has ended. Exit by pressing the ESC key.

Input: ESC-key

Printer response:

\$

CI :

5. Input: P SERL (CR)

Printer response:

CISERL:

6. Input: X (CR)

Printer response:

X.
00[FFM TCM TIM ROL]

CISERL:

7. Input: ESC-key

Printer response:

\$

CI :

8. Input: P LGTS (CR)

Printer response:

CILGTS:

9. Input: X (CR)

Printer response:

X.

00[LGT

Light A should be on.

Press RETURN key to continue.

10. Verify that only Error Light A is on before proceeding.

11. Input: (CR)

Printer response:

Light B should be ON.

Press RETURN key to continue.

12. Verify that only Error Light B is ON before proceeding.

13. Input: (CR)

Printer response:

Light X should be ON.

Press RETURN key to continue.

14. Verify that only Error Light X is ON before proceeding.

15. Input: (CR)

Printer response:

]

CILGTS:

16. Input: ESC-key

Printer response:

\$

CI :

17. Input: P SMMC (CR)

Printer response:

CISMMC:

18. Input: X (CR)

Printer response:

X.

00 [SMM]

CISMMC:

19. The CTSI CCA diagnostic test is complete. If no errors were reported by MADTS, the assembly is good.

20. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 11.7 and Table 11-1, CTS Interface Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the MIFC FSAS Equipment Instruction Book (TI 6490.37) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

11.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Disconnect cable P/N 401-37876-01, P1 from J3 on the CTSI, and P2 from DRV11-J, J2. Disconnect cable P/N 401-37849-01, P2 from CTSI J2, P3 from CTS TEST, and P1 from DRV11-J J1. Disconnect cable P/N 401-37126-07, P1 from CTS J1, and P2 from Channel 2 on MADTS TMI 8S Ports.
4. Remove DRV11-J CCA from extender board.

5. If another CTS Interface assembly is to be tested, return to paragraph 11.4 and proceed.
6. Remove extender board from Electronics Chassis card cage.
7. Replace System DRV11-J CCA into slot A1-L4.

11.7 MADTS CTS INTERFACE LIGHT DIAGNOSTIC PROGRAM.

11.7.1 Function Mnemonics. The test function mnemonics used by the CTS Interface Light diagnostic program are given below. Unless otherwise noted, functions are enabled by default for the manual test mode and disabled during the automatic test mode. This diagnostic requires that a DRV11-J parallel interface be connected to both CTS time inputs using a special cable harness.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
LGT	Lights each of the error lights on the CTS interface panel.

11.7.2 Function Stimuli Descriptions. The CILGTS diagnostic program contains no stimuli. It is used to sequentially illuminate lights A, B, and X on the CTS interface panel to allow the MADTS specialist to verify that the lights are operating correctly.

11.8 MADTS CTS INTERFACE SMMC DIAGNOSTIC PROGRAM.

11.8.1 Function Mnemonics. The test function mnemonics used by the CTS Interface SMMC diagnostic program are enabled by default for the manual test mode and disabled during automatic test mode. This diagnostic requires that a DRV11-J parallel interface be connected to both CTS time input using a special cable harness.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
SMM	Ensures that the CTS interface is performing its SMMC light function successfully.

11.8.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected by the MADTS specialist. The stimuli for each function and associated error data are as follows.

11.9 MADTS CTS INTERFACE PARALLEL DIAGNOSTIC PROGRAM

11.9.1 Function Mnemonics. The test function mnemonics used by the CTS Interface Parallel diagnostic program are given below. Functions are enabled by default for the manual test mode. The program automatically determines if the DRV11-J parallel interface is responding. A negative result is reported in both the manual and automatic mode.

<u>Mnemonic</u>	<u>Function</u>
a. BIN	Ensures that the 30 parallel lines of both time inputs are functioning correctly
b. LTX	Alters the parallel line input to cause an X type error
c. LAX	Alters the parallel line input to cause an A and an X type error
d. LBX	Alters the parallel line input to cause a B and an X type error
e. ABX	Alters the parallel line input to cause an A, a B, and an X type error

11.9.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which may result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected by the MADTS specialist. The stimuli for each function and associated error data are given below. The diagnostic requires that a DRV11-J parallel interface be connected to both CTS time inputs using a special cable harness.

11.10 MADTS CTS INTERFACE (SERIAL) DIAGNOSTIC PROGRAM.

11.10.1 Function Mnemonics. The test function mnemonics used by the CTS Interface Serial diagnostic program are listed below. Functions are enabled by default for the manual test mode. The program automatically determines if the DRV11-J parallel interface is responding. A negative result is reported in both the manual and automatic mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. FFM	Ensures that the F (format) command function of the CTS interface is operating correctly.
b. TCM	Ensures that the T (send time) command function of the CTS interface is operating correctly.
c. TIM	Ensures that a time can be correctly output by the CTS interface. Enabled for the automatic confidence check.
d. ROL	Ensures that the CTS interface can correctly handle times that rollover to minute 1, hour 1, and day 1.

11.10.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 11-1.

11.11 MADTS CTS ERROR OUTPUT FORMAT.

Error codes and any associated data are output in the form:

ERROR #xxxx aaaaaa bbbbbb

where:

xxxx is the error number
 aaaaaa is an output parameter
 bbbbbb is an output parameter

The number of output parameters can vary from zero to two depending on the error. Additional error data may be given in an annotated dump format as shown below:

Expected CTS output:

000000 000001 001004 004020 020100 000100

Actual CTS output:

000000 000000 000000 000000 000000 000000

The error codes used by the MADTS CTS Interface diagnostic program and their associated output parameters are given in Table 11-1.

Table 11-1. CTS Interface Diagnostic Error Message Description
(LGTS)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LGT	NONE	The CTS interface is initialized with a time. The time +1 second is sent over line #2, which causes light A to illuminate. The specialist must verify the illumination of the light and press return to continue. The interface is re-initialized before the time +1 second is sent over line #1, causing light B to illuminate. The specialist must verify the illumination of the light and press the return key to continue. The interface is re-initialized before the time +2 seconds is sent over line #1 and the time +3 seconds is sent over line #2. This causes light X to illuminate. The specialist must verify the illumination of the light and press the return key to continue. The interface is then reset.	NONE	NONE	NONE

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(SMMC)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SMM	SMMC Light On Test	A command is sent to the CTS interface which will cause it to turn on the SMMC light. The interface is given a time which is then output over the serial line. The output string contains a status indicator which is verified in order to ensure that the SMMC light-on command was properly recognized. An indicator of 1 is expected.	0	The SMMC light would not turn on when the light-on command was sent to the CTS interface board.	Actual light status indicator
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read. Previous characters read, if any.
	SMMC Light Off Test	A command is sent to the CTS interface which will cause it to turn off the SMMC light. The interface is given a time which is then output over the serial line. The output string contains a status indicator which is verified in order to ensure that the SMMC light-off command was properly recognized. An indicator of 0 is expected.	2	The SMMC light would not turn off when the light-off command was sent to the CTS interface board.	Actual light status indicator
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read. Previous characters read, if any.

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
BIN	Line 1 and 2 Binary Test	The CTS interface is initialized with a time which has only bit #1 set. The time +1 second is sent to the interface over both parallel time inputs. No error lights should illuminate. The resulting output string includes a light status indicator which is verified to insure that the time inputs are operating correctly. The sequence repeats with the set bit being left shifted one place for each iteration until bits 1 to 29 have been tested.	0	The CTS interface light state indicator received over the serial line indicates a state different than what was expected. See Table 11-2 for the status and their meaning.	Expected Status indicator Actual Status indicator Parallel data sent to the CTS Interface.
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters read (if any)
	Line 1 Binary Test	The CTS interface is initialized with a time which has only bit #1 set. The time +1 second is sent to the interface over time input #1. Error light 'B' should illuminate. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly. The sequence repeats with	0	The CTS interface light state indicator received over the serial time indicates a state different than was expected. See Table 11-2 for the status and their meaning.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS Interface
			10	The CTS interface board did not output a character over the serial line.	Number of characters read Previous characters that were read (if any)

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRLI)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
Line 2 Binary Test		the set bit being shifted left one place for each iterations until bits 1 through 29 have been tested.		Within the allowable time.	
		The CTS interface is initialized with a time which has only bit #1 set. The time +1 second is sent to the interface over time input #2. Error light 'A' should illuminate. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating properly. The sequence repeats with the set bit being left shifted one place for each iteration until bits 1 through 29 have been tested.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table 11-2 for the light states and their meaning.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS Interface
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
LTX	Error 'X' Binary Test	The CTS interface is initialized with a time. The time +2 seconds is sent to the interface over time input #1. The original time +3 seconds is sent over time input #2. Only	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table	Expected light status indicator Actual light status indicator Parallel data sent to the CTS interface.

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LAX		error light 'X' should illuminate. The resulting output string includes a light status indicator which is verified to insure that the time inputs are operating correctly.	10	11-2 for the states and their meaning. The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
		The CTS interface is initialized with a time. The time +1 second is sent to the interface over time input #2. Only error light 'A' should illuminate. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS interface.
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
	Error 'X' Binary Test	The time +3 seconds is sent to the interface over time input #2. Only error lights 'A' and 'X' should be illuminated. The resulting output string includes a light status indicator which is verified to ensure that the time	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS interface.
			10	The CTS interface	Number of characters

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LBX	Error 'B' Binary Test	inputs are operating correctly.		board did not output a character over the serial line within the allowable time.	read Previous characters that were read (if any)
		The CTS interface is initialized with a time. The time +1 second is sent to the interface over time input #1. Only error light 'B' should illuminate. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS Interface.
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
		The time +3 seconds is sent to the interface over time input #1. Only error lights 'B' and 'X' should be illuminated. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS Interface.
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ABX	Error 'A' Binary Test	The CTS interface is initialized with a time. The time +1 second is sent to the interface over time input #2. The original time +1 hour is sent to the interface over time input #1. Only error light 'A' should illuminate. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Parallel data sent to the CTS interface. Number of characters read Previous characters that were read (if any)
	Error 'X' Binary Test	The existing time +1 second is sent to the interface over time input #1. The time +1 hour is sent to the interface over time input #2. Only error lights 'A' and 'X' should be illuminated. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light status indicator received over the serial line indicates a state different than was expected.	Expected light status indicator Actual light status indicator
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Parallel data sent to the CTS interface Number of characters read Previous characters that were read (if any)

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(PRL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
Error 'B' Binary Test		The existing time +1 second is sent to the interface over time input #2. The time input -1 hour is sent to the interface over time input #1. Error lights A, B, and X should be illuminated. The resulting output string includes a light status indicator which is verified to ensure that the time inputs are operating correctly.	0	The CTS interface light state indicator received over the serial line indicates a state different than was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator Parallel data sent to the CTS interface.
			10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(SERL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
FFM	Format Test	A format of DDD:HH:MM:SS SQ is sent to the CTS interface. The interface is initialized with a time. A second format command is sent which instructs the interface to use a format of DDD/99:MM:SS Q. The time +1 second is sent to the interface over line #1 which results in the time being output in the new format. The output string is then verified for proper content and format.	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			8	The time string output by the CTS interface board is incorrectly formatted.	Expected time string Actual time output
TCM	'T' Command Test	The CTS interface is initialized with a time. The 'T' command is sent to the interface. The time +1 second is sent over line #1, causing the time to be output. The time is verified and the interface returned to its normal mode ('C' mode).	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			6	The time that was output by the CTS interface over the serial line does not match what was expected based on the parallel time which was input.	Expected time string Actual time string

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(SERL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
TIM	Time Output Test	The CTS interface is initialized with a time. The time +1 second is sent to the interface over both time input lines. The resulting time output is read and verified.	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			4	The CTS interface light state indicator received over the serial line indicates a state different from what was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator
			6	The time that was output by the CTS interface does not match what was expected based on the parallel time input.	Expected time string Actual time string
ROL	Minute Rollover Test	The CTS interface is initialized to a time of 000:00:00:58. The time +1 second is sent to the interface over both time input lines. The time output is read and verified. The time is again incremented	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			4	The CTS interface light state indica-	Expected light status indicator

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(SERL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		by one and sent to the interface, causing the time to roll over to minute 1. The time is again read and verified.		tor received over the serial line indicates a state different from what was expected. See Table 11-2 for the states and their meaning.	Actual light status indicator
			6	The time that was output by the CTS interface does not match what was expected based on the parallel time input.	Expected time string Actual time string
Hour Rollover Test		The CTS interface is initialized to a time of 000:00: 59: 58. The time +1 second is sent to the interface over both input lines. The time output is read and verified. The time is again incremented by one and sent to the interface, causing the time to roll over to hour 1. The time is again read and verified.	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			4	The CTS interface light state indicator received over the serial line indicates a state different from what expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator
			6	The time that was	Expected time string

Table 11-1. CTS Interface Diagnostic Error Message Description (Continued)
(SERL)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
				output by the CTS interface does not match what was expected based on the parallel time input.	Actual time string
Day Rollover Test		The CTS interface is initialized to a time of 000:23: 59: 58. The time +1 second is sent to the interface over both time input lines. The time output is read and verified. The time is again incremented by one and sent to the interface, causing the time to roll over to day 1. The time is again read and verified.	10	The CTS interface board did not output a character over the serial line within the allowable time.	Number of characters read Previous characters that were read (if any)
			4	The CTS interface light state indicator received over the serial line indicates a state different from what was expected. See Table 11-2 for the states and their meaning.	Expected light status indicator Actual light status indicator
			6	The time that was output by the CTS interface does not match was was expected based on the parallel time input.	Expected time string Actual time string

Table 11-2 CTS Interface Light State Indications

- 0-All lights and SMMC are off
- 1-SMMC is on
- 2-Light A is on
- 3-SMMC and light A are on
- 4-Light X is on
- 5-SMMC and light X are on
- 6-Light A & X are on
- 7-SMMC and lights A and X are on
- 8-Light B is on
- 9-SMMC and lights B are on
- 5-Lights A, B, and X are on
- 4-Lights B and X are on
- 4-Lights C and X are on
- 4-Lights A and B are on

SECTION XII LRU TEST PROCEDURES KEYBOARD UNIT P/N 401-36735

12.1 GENERAL. This section contains the test procedures for the E-Systems Keyboard Unit P/N 401-36735, as tested by the MADTS. The test is conducted under diagnostic software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

12.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Keyboard:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
Maintenance and Diagnostic Test Set (MADTS)	E-Systems P/N 401-37570
Keyboard Test Power Cable	E-Systems P/N 401-37865-01
Keyboard Interconnect Cable	E-Systems P/N 401-36738-01

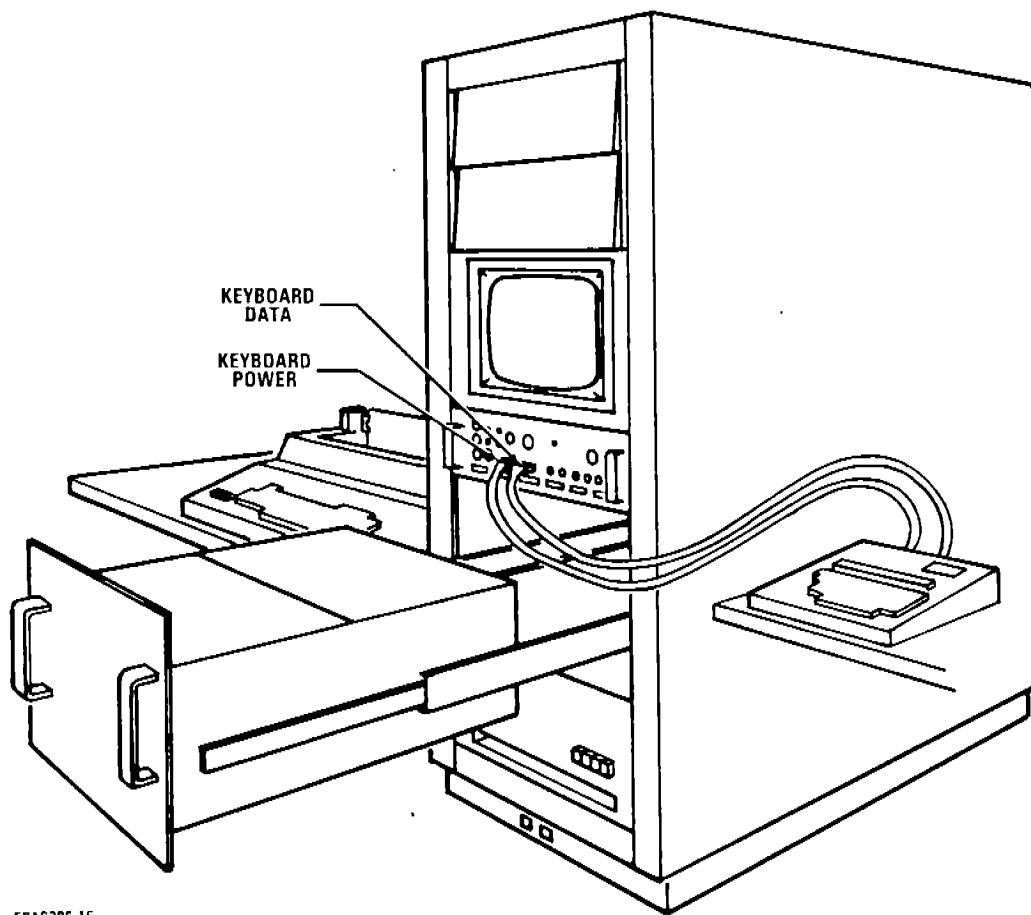
Tools other than standard shop tools are not required for test.

12.3 OTHER DOCUMENTATION. Other documentation required for test is the Instruction Book, Keyboard Unit (TI 6490.16), and the M1FC FSAS System Instruction Book (TI 6490.36).

12.4 PREPARATION FOR TEST. To prepare the Keyboard Unit for test by the MADTS, follow the instructions listed below and see Figure 12-1.

1. Verify that system power switch is in ON position.
2. Set Electronics Chassis Power switch to OFF.
3. Connect test cable P/N 401-37865, P1 to KEYBOARD POWER on I/O Control Panel and connect other end of cable, P2 to J2 on back of Position Keyboard under test.
4. Connect test cable P/N 401-36738-01, P1 to KEYBOARD DATA on I/O Control Panel and connect other end of cable, P2 to J1 on back of Position Keyboard under test.

12.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:



FSAS306-16

Figure 12-1. ESY Keyboard Test Set-Up

Printer response:

While pressing the control (CNTRL) key press the A key

6. Press the control key, hold and press the A key.

Printer response:

While pressing the left SHIFT key, press the 1 key.

7. Press the left SHIFT key, hold and press the 1 key.

Printer response:

D

While pressing the right SHIFT key, press the 5 key

8. Press the right SHIFT key, hold and press the 5 key.

Printer response:

Set KEYBOARD selection to desired channel

Press "C" key to continue or "E" to exit

9. Set KEYBOARD OUTPUT SELECT switch on the I/O Control Panel to Channel 2. Repeat steps 4 through 9 for channel 2.
10. The Position Keyboard Unit diagnostic test is complete. If no errors were reported by MADTS, the Keyboard is good.
11. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to Table 12-1, Keyboard Error Messages. This table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the Keyboard Unit Instruction Book (TI 6490.16) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).
12. If additional keyboards are to be tested press the E key.

Printer response:

ECH

Set keyboard selector to desired channel

Press the C key to continue or the E key to exit.

13. Input: E

Printer response:

KBDIAG:

14. Return to step 2 and continue testing.

12.6 POWER DOWN SEQUENCE

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Disconnect cable P/N 401-36738-02, P2 from J1 on Position Keyboard under test.
4. Disconnect cable P/N 401-37865, P2 from J2 on Position Keyboard under test.
5. Disconnect cable P/N 401-36738-02, P1 from KEYBOARD DATA on I/O Control Panel.
6. Disconnect cable 401-37865, P1 from KEYBOARD POWER on I/O Control Panel.

2
@
SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D KB (CR)

Printer response:

KBDIAG:

2. Input: X (CR)

Printer response

X.

00[KEY

SET KEYBOARD selector to desired channel

Depress "C" Key to continue or "E" to exit

3. Set KEYBOARD OUTPUT SELECT switch on the I/O Control Panel to 1.

4. Input: C

Printer response:

With SHIFT LOCK off depress the following key sequences:

PG FWD to MPB

PG RVS to ENTER

DELETE to LINE INSERT

Q to CHAR INSERT

A to RIGHT ARROW (include CR)

Z to CLEAR (skip CR) and space bar

5. Verify that the shift lock key is OFF. Depress each key on the Position Keyboard in the order specified above. The DEC LA34/LA100 console will echo print all printable characters as they are typed.

Table 12-1. Keyboard Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
KEY	Caps-lock key test	A message is output to the console giving the operator test instructions which include releasing the CAPS-LOCK key and typing keys on the keyboard, going from left to right and top to bottom. The keys must be typed in the indicated sequence. Displayable characters typed are echoed to the console. After the sequence has been completed, any errors are reported. If a key is not typed within 5 minutes, the function is terminated with any accumulated errors reported.	18	One or more character codes do not match those in the pre-determined key sequence.	Annotated dump consisting of: Relative key number. Expected key code. Actual key code.
	Control Key Test	A message is output to the console instructing the operator to type the control and 'A' keys simultaneously. The resulting keycode is verified. If a key is not typed within 5 minutes, the function is terminated.	4	A parity error occurred during receipt of a serial character from the device.	CSR contents (BFD)

Table 12-1. Keyboard Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			6	An overrun error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			14	A character code other than control-A (SOH) was received.	Expected character actual character
Shift Key Test		A message is output to the console instructing the operator to press the Shift and '1' keys simultaneously. The resulting key-code is echoed to the console and verified. A message is then output to the console which instructs the operator to press the Shift and '5' keys simultaneously. The resulting key-code is then echoed and verified. If a key is not pressed within 5 minutes, the function is terminated.	4	See previous error #4 text.	
			6	See previous error #6 text.	
			8	See previous error #8 text.	
			16	An invalid shifted character was received.	Expected character actual character

Table 12-1. Keyboard Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ECH	Echo Character	Each key on the position keyboard which is pressed is echoed to the console. Non-displayable key-codes will have their octal value printed. Pressing the Delete key before any key will cause that key's octal value to be printed. If a key is not pressed within 5 minutes, the function is terminated.	4	See previous error #4 text.	
			6	See previous error #6 text.	
			8	See previous error #8 text.	

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FEDERAL AVIATION ADMINISTRATION

6490.16 CHG 14

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ELECTRONIC EQUIPMENT MODIFICATION HANDBOOK
✓ SUBJ: FLIGHT SERVICE AUTOMATION SYSTEM

CHAPTER 13. REPLACEMENT OF THE COMMUNICATION PROCESSOR
8S CARD WITH 4S CARD AT AUTOMATED FLIGHT
SERVICE STATIONS
FA-10018

1. PURPOSE. This chapter authorizes a modification to the automated flight service station (AFSS) communication processor (CP) equipment by replacing the serial communications card, model number TMI-8S, with model number DLV11-J (4S card).
2. DISTRIBUTION. This directive is distributed to selected offices and services within Washington headquarters, regional Airway Facilities divisions, the FAA Technical Center, the Mike Monroney Aeronautical Center, and the Airway Facilities field offices having the following facilities/equipment: AFSS
3. WITHDRAWALS. Not applicable.
4. REFERENCES.
 - a. Configuration Control Decision N15794.
 - b. Model 1 Full Capacity Flight Service Automation System TI 6490.37, Instruction Book.
5. BACKGROUND. The current TMI-8S card is one of the selective hardware components at the AFSS nearing depletion in logistics support. By replacing the 8S card with a DLV11-J 4S card in the CP equipment, freed-up TMI-8S cards will alleviate a potential shortage problem.
6. APPLICATION. This modification is applicable to all AFSS sites.

Distribution: Selected Airway Facilities Field
and Regional Offices; ZAF-600

Initiated By: AOS-540

45 13-1

6490.16 CHG 14

7. MATERIALS REQUIRED. The materials required to perform this modification consist of the following:

<u>ITEM</u>	<u>DESCRIPTION</u>	<u>NSN/PART NUMBER</u>	<u>QUANTITY</u>
a.	DEC Serial Interface cards	5998-01-072-1568	4 each (including 1 spare)
b.	Interface cables	6150-01-416-4024	3 each

8. SOURCE OF MATERIALS. The materials required are readily available from the FAA Logistics Center (FAALC) and must be ordered by each facility via normal requisition procedures.

9. SPECIAL TOOLS AND TEST EQUIPMENT REQUIRED. Not applicable.

10. MODIFICATION TO BE PERFORMED BY. This modification is to be performed by field maintenance personnel or as determined by the regional Airway Facilities division manager.

11. WHEN MODIFICATION IS TO BE PERFORMED. This modification is to be performed as soon as possible after receipt of this chapter and the required material.

12. ESTIMATED TIME REQUIRED. This modification will require one technician for 1.0 employee-hour.

13. DISPOSITION OF SURPLUS PARTS. The three removed TMI-8S cards should be immediately shipped to the FAALC at the following address:

FAA Logistics Center
6500 South MacArthur
P.O. Box 25082
Oklahoma City, OK 73125
ATTN: RECEIVING DOCK, Mark for Operating Stock

If any problems arise in disposing of this material, site personnel should contact the Flight Service Branch, AOS-540 at (609) 485-HELP.

14. MODIFICATION PROCEDURE. REPLACEMENT OF THE COMMUNICATION PROCESSOR 8S CARD WITH 4S CARD AT THE AFSS.

ADDITIONAL BACKGROUND INFORMATION

In the Flight Service Automation System (FSAS) application, the TMI-8S serial communications card is utilized in one of four configurations; Serial-I/O, Keyboard #1, Keyboard #2, and MADTS. In this procedure, the Serial-I/O configured card in CP will be exchanged for a DEC DLV11-J serial-I/O card.

Due to a unique interface connector used by the DLV11-J, a special cable must be utilized. Appendix A illustrates the data flow between the LSI-11 bus for each of the three CPs, and the Input/Output Terminal (IOT) console.

OVERVIEW OF PROCEDURE

These steps will allow online replacement of the Serial-I/O cards in each of the three CPs without an outage of the AFSS facility. A small screwdriver and wirewrap tool will be required for this procedure.

PRELIMINARY STEPS

- a. Set the IOT console power on and the left-hand keyboard buttons set for online and 300 baud.
- b. Verify that the IOT console is functional via the existing paths to CP#0, CP#1, and CP#2. This will require a patch cable for CP#1 and CP#2. Refer to figure 1 for patch panel plug locations. For CP#1, patch from "x" to "y." For CP#2, patch from "x" to "z."

	IOT	NC	NC	NC
CPU	x	o	o	o
MODEM	o	y	z	o
MON	o	o	o	o
	CP#0	CP#1	CP#2	PP#0

FIGURE 1. PART OF AFSS DIGITAL PATCH PANEL 1A4, FRONT VIEW

- c. Verify that all required components are available and configured correctly as indicated:
 - (1) Four DEC DLV11-J serial interface cards, consisting of three cards to be installed and one to be configured, tested, and saved as a site spare. Verify that all four cards are configured to even parity enabled for the channel 3 (console) communication line parameters as illustrated in appendixes B and C.
 - (2) Three 8-foot interface cables, one for each CP. The cables should be labeled approximately six inches from both ends with the following digital patch panel (1A4) information:
 - (a) W935A 1A4-A1J2 CP#0 SERIAL-I/O J3.
 - (b) W942A 1A4-A2J2 CP#1 SERIAL-I/O J3.
 - (c) W923A 1A4-A3J2 CP#2 SERIAL-I/O J3.

REPLACEMENT PROCEDURE

- a. At the front of cabinet 2, open the front door panel and leave open for the duration of this procedure.
- b. At the rear of cabinet 1, at Patch Panel A4, disconnect cable connections W935 (at A4A1J2), W942 (at A4A2J2), and W923 (at A4A3J2). Note that cable W701 at A4A1J1 to the IOT console and the remaining J2 cables to each Position Processor will not be removed.
- c. Install the DB25F connector of each interface cable to the locations specified:
 - (1) W935A to 1A4 patch panel A1J2 for CP#0.
 - (2) W942A to 1A4 patch panel A2J2 for CP#1.
 - (3) W923A to 1A4 patch panel A3J2 for CP#2.
- d. Route the other end of all three cables to the front of the system between cabinets 1 and 2 towards the open front door panel of cabinet 2.
- e. At the AFSS Supervisory FCOTC position or at the Flight Service Data Processing System (FSDPS) FCOTC position, each CP must be placed offline, one at a time, during the serial interface card replacement. To do this, first use the command CF <Enter>. Next press TAB to the desired CL (Communications Line) assignment. Type in either 0, 1 or 2 so that the two CPs not being worked on each have two communications lines assigned. Then press HOME and type CP <Enter> CD <Enter>. This will leave the desired CP in an "I" status. Use the CF <Enter> again to confirm the status of the CP.

NOTE: Refer to door panel plate #401-37999-03 to confirm location of each CP and each serial interface card. Note that the cabinet coordinates 2A4 contains CP#0 and CP#1, and location 2A5 contains CP#2.

- f. Once the selected CP is out of service, switch power to the "OFF" position for that CP.
- g. With the selected CP now powered off, locate the existing "Serial-I/O" card. This is situated in the following locations:
 - (1) 2A5-A2-4 Lower, for CP #0. (Item H on door diagram.)
 - (2) 2A5-A4-3 Lower, for CP #1. (Item S on door diagram.)
 - (3) 2A4-A2-4 Lower, for CP #2. (Item H on door diagram.)

- h. Remove the 40-pin cable connector at the serial card.
- i. Remove the TMI-8S serial card from the system.
- j. Install the DLV11-J serial card into the same card slot.
- k. At the bottom connector of the new serial card, location J3, install the appropriate interface cable connector for that CP. Observe the key polarity of the connector.
- l. If other than CP#0, install a digital patch panel cable between the IOT and the CP which has just been modified. Refer to figure 1 for patch panel locations. For CP#1 patch from "x" to "y." For CP#2 patch from "x" to "z" as shown in figure 1.
- m. Apply power to the CP. Confirm that the normal startup printout appears, as shown below, where "n" is the CP number. This process takes about 70 seconds from the time of applying power.

```

SELFTEST [ CPU RAM REF PAT ADR MMU CPY XFR INT XMM ]
n:LOADING CP OPERATIONAL S/W
CP LOAD COMPLETE

```

n:

- n. Restore the offline CP to service. At the AFSS Supervisory FCOTC position or at the FSDPS FCOTC position, each CP must be placed offline, one at a time, during the serial interface card replacement. To do this, use the CF <Enter> command then TAB to the CL assignments. Type in either 0 1 or 2 to restore all CPs to service. Then press HOME then type CP <Enter> CD <Enter>.

NOTE: It is highly recommended that all three CPs be back in service for at least two minutes prior to removing the next CP from service for modification.

Repeat this procedure for each CP until all have been modified. At the option of the technician, the fourth DLV11-J card may be installed and tested prior to returning the AFSS to full operation.


- o. Upon completion of this procedure, three cables with part number 401-37126-01, connected to J4 of each Mux Interface Assembly, will no longer be in use and may be left inside the rear of cabinet 2. Also in cabinet 2, three cables which are part of each Mux Interface Assembly should be coiled and stored neatly.

7/10/95

- p. The three removed TMI-8S cards are to be immediately shipped to the FAA Depot using the following address on the mailing label:

FAA Logistics Center
6500 South MacArthur Blvd
P.O. Box 25082
Oklahoma City, OK 73125
ATTN: RECEIVING DOCK, Mark for Operating Stock

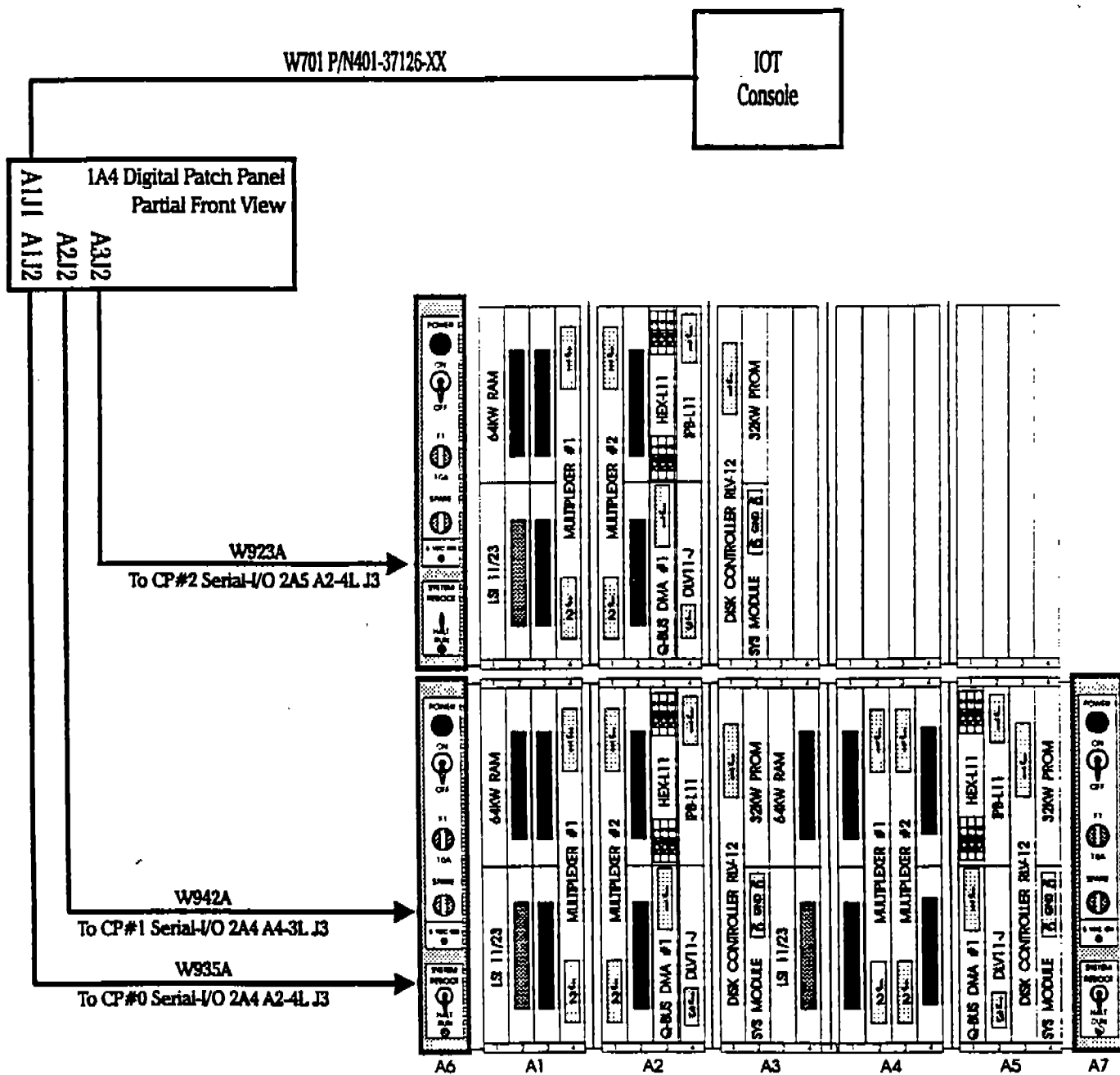
15. TEST AFTER MODIFICATION. Reconfigure the CP equipment online in a test environment. Initiate the software to bring all sites back online. From the system supervisor terminal (SST), independently reconfigure each communication line Offline then back Online. Ensure normal communication line reconfigurations.
16. RESULT OF MODIFICATION. This modification will result in a sufficient quantity of selective spare components to support the AFSS through its planned life cycle.
17. CHANGES TO INSTRUCTION BOOKS. Not applicable.
18. CHANGES TO INSTALLATION DRAWINGS. Not applicable.
19. CHANGES TO RECORDED DATA. Prepare FAA Form 6032-1, Airway Facilities Modification Record, showing this directive number, date, chapter and change number to change recorded data.
20. CHANGES TO TABLE OF CONTENTS. This chapter will be included in the next revision of the table of contents for this handbook.
21. RECOMMENDATIONS FOR CHANGES. Forward any recommendations for changes to this directive through normal channels to the National Data Communications Systems Engineering Division, AOS-500, Operational Support.
22. SOFTWARE IMPACT. Not applicable.
23. STATUS ACCOUNTING. Ensure that the Quarterly NAS Equipment and EEM Status Report is updated to indicate the installation of this modification.


George W. Terrell

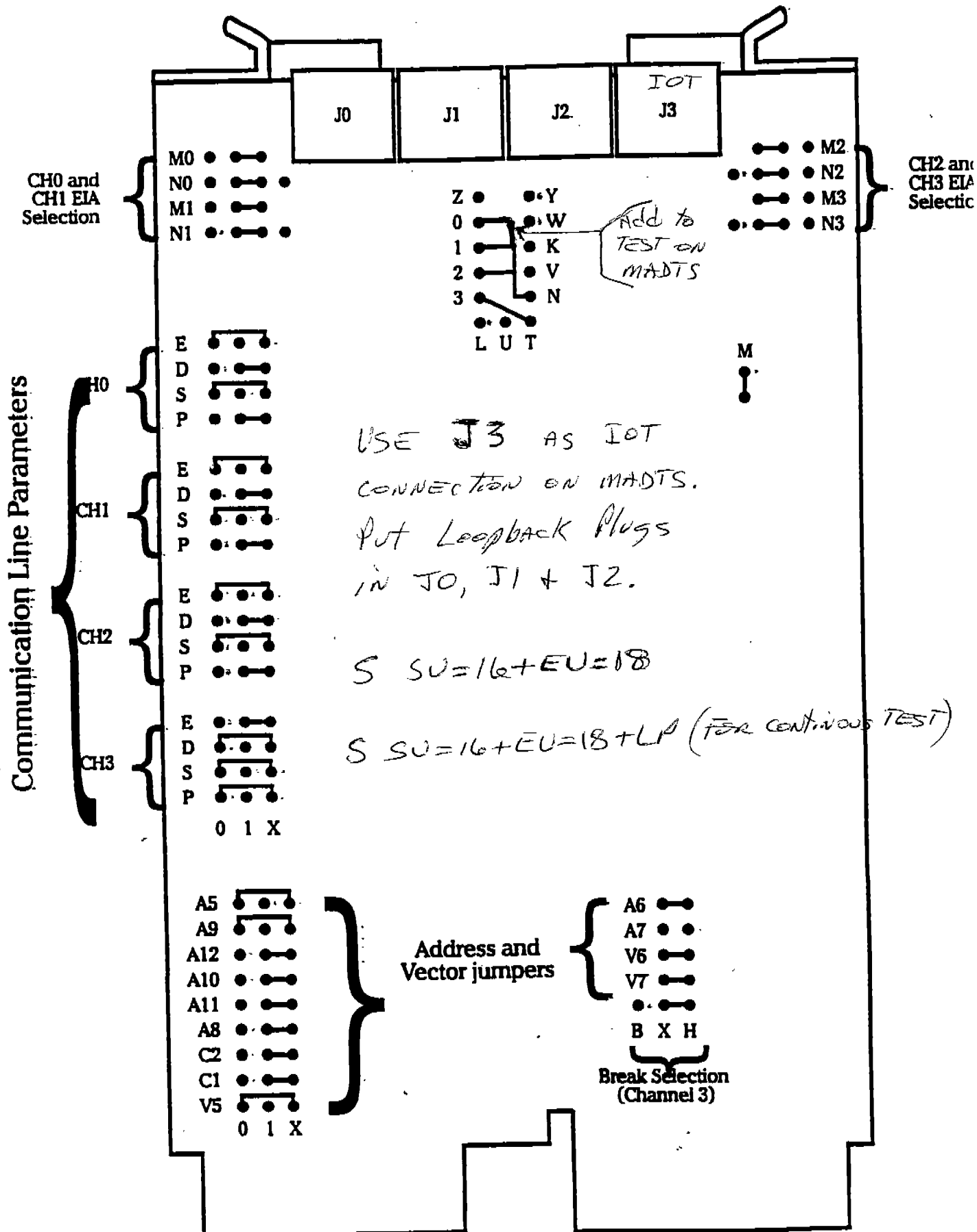
Program Director for Operational Support

4 Appendixes

APPENDIX A. AFSS IOT CONSOLE DATA FLOW



APPENDIX B. DLV11-J SERIAL INTERFACE CARD



APPENDIX C. DLV11-J JUMPER CONFIGURATION**Address and Vector Jumpers (176500 vector 300)**

A5	X to 0	A6	installed
A9	X to 0	A7	open
A12	X to 1	V6	installed
A10	X to 1	V7	installed
A11	X to 1		
A8	X to 1		
C2	X to 1		
C1	X to 1		
V5	X to 0		

Break Selection

B	X	H	X to H
---	---	---	--------

Channel 0 through 2 Characteristics

E,D,S,P	Not used
---------	----------

Channel 3 (Console) 7 data bits, 1 stop bit, even parity enabled

E	X to 1	Even Parity
D	X to 0	7 data bits
S	X to 0	1 stop bit
P	X to 0	Parity Enabled

Baud Rate Selection

0,1,2	Not used
3	3 to T 300 baud

Cable Connector Information

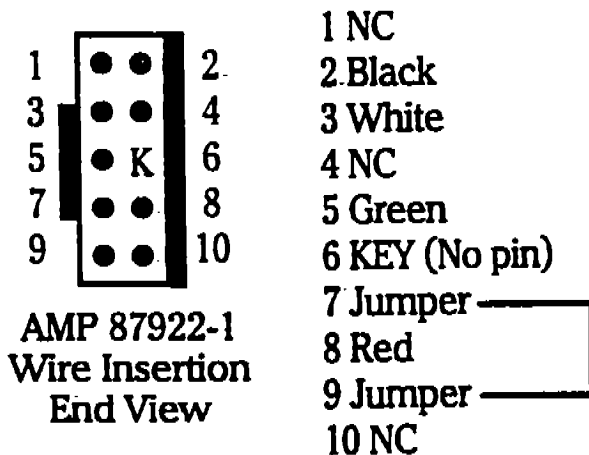
AMP #87133-5	Cable receptacle
AMP #87124-1	Locking clip contacts (optional)
AMP #87179-1	Key pin (pin 6, optional)
AMP #87922-1	Cable plug

Cable Pin Assignments

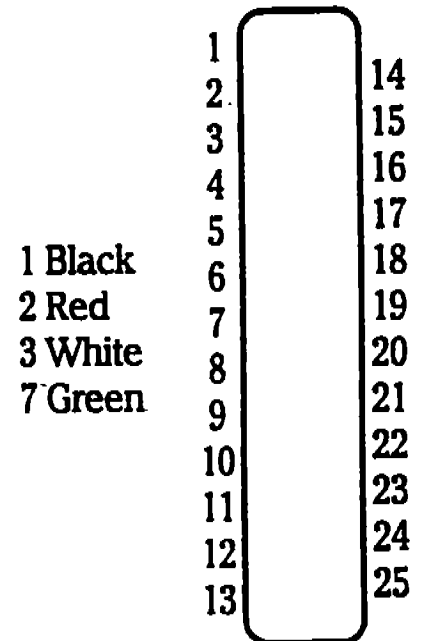
DLV11-J		DB-25F
2	to	1
3	to	3
5	to	7
6	Key	
7 to 9	jumper	
8	to	2
9 to 7	jumper	

APPENDIX D. DLV-RS232 CABLE

Connector #1
AMP #87922-1
5 x 2 pins



Connector #2
Generic DB-25 Female
Data Connector with
Cover and 2 screws



Notes:

- Each cable is 8 feet long.
- Connector #1 is AMP #87922-1, a 10-pin double-row (5 x 2) connector.
A "key" should be in position #6 for polarity.
- Cables are in sets of three (3) with each end labeled as shown.

Cable "W935A":

Near DB-25: W935A 1A4-A1J2 CP#0

Near AMP: W935A CP#0 Serial I/O J3

Cable "W942A":

Near DB-25: W942A 1A4-A2J2 CP#1

Near AMP: W942A CP#1 Serial I/O J3

Cable "W923A":

Near DB-25: W923A 1A4-A3J2 CP#2

Near AMP: W923A CP#2 Serial I/O J3

13 18

23 28

SECTION XIII
LRU TEST PROCEDURES
8S SERIAL INTERFACE
(COMMUNICATIONS CONFIGURATION)
(KEYBOARD CONFIGURATION)

13.1 GENERAL. This section contains test procedures for the 8S Serial Interface CCA as tested on the MADTS. The 8S CCA may be configured as a Communications Interface or as a Keyboard Interface. The configuration is dependent upon strapping. Either configuration may be tested by MADTS.

13.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the 8S Serial Interface:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
MADTS	E-Systems P/N 401-37570-01
Test Cable	E-Systems P/N 401-37863
Test Cable, (2 each)	E-Systems P/N 401-37864
Standard Dual Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test of the 8S Serial Interface.

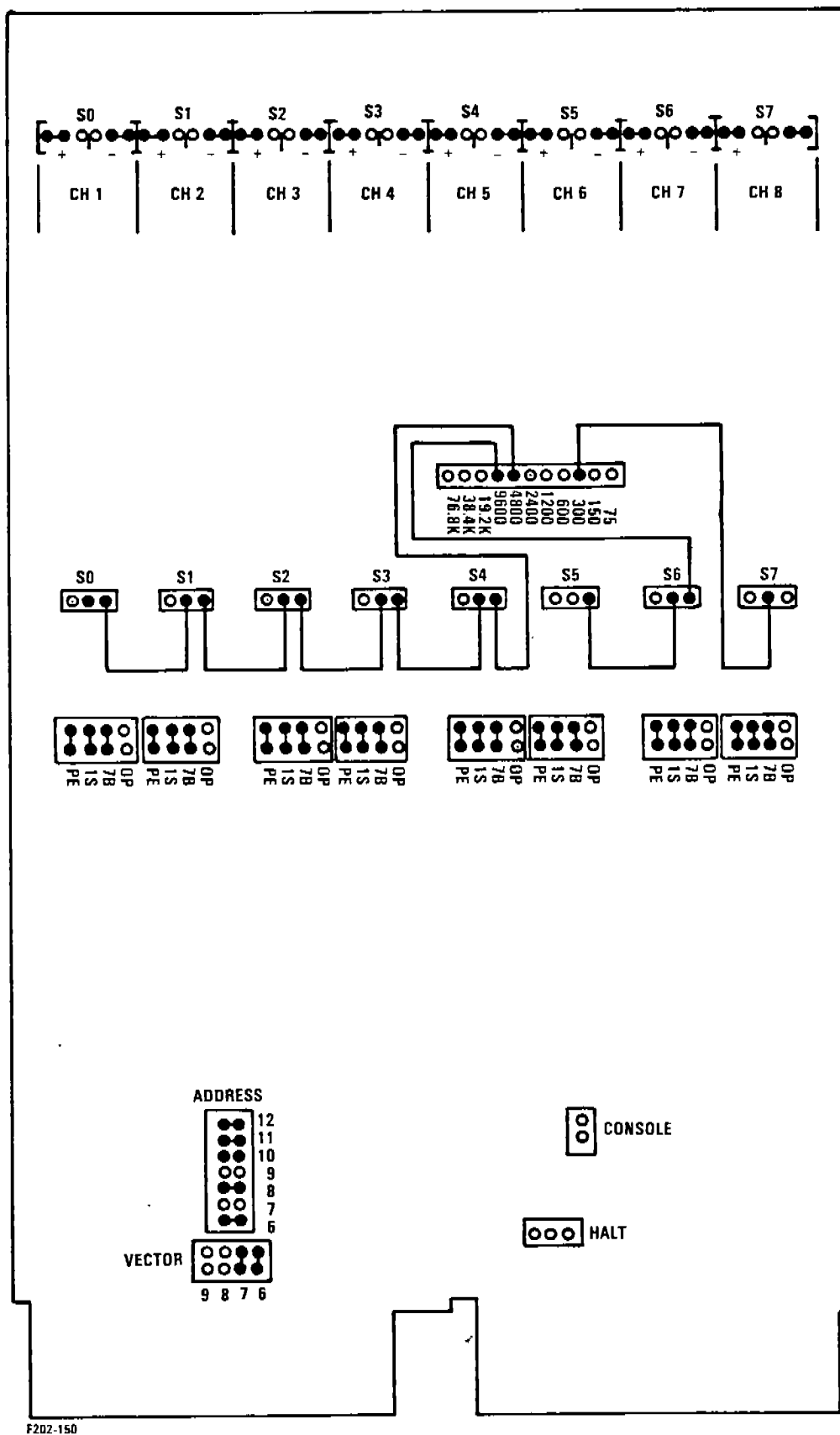
13.3 OTHER DOCUMENTATION. The only other documentation required for test or troubleshooting the 8S Serial Interface is the Eight Channel Serial Instruction Book, TI 6490.9. Refer to this manual for detailed information on theory of operation and schematic diagrams.

13.4 PREPARATION FOR TEST. To prepare the 8S Serial CCA for test, follow the instructions listed below.

1. Inspect 8S Serial CCA (unit to be tested) and determine if it is configured as communications interface or keyboard interface. If CCA has CONSOLE jumper removed, it is communications interface or if CONSOLE jumper is installed, then CCA is keyboard interface. See Figure 13-1 and Figure 13-3.
2. Inspect 8S CCA (unit to be tested) to ensure that it is configured as in Table 13-1, Communications Configuration, or that it is configured as in Table 13-2, Keyboard Configuration.

NOTE

For Communication Configuration proceed to paragraph 13.5. For Keyboard Configuration proceed to paragraph 13.6.



F202-150

Figure 13-1. 8S Communications Configuration

Table 13-1. TMI 8S Communication Configuration - Serial I/O

A12	Installed	}	Strapped for Device Address 776500
A11	Installed		
A10	Installed		
A 9	Removed		
A 8	Installed		
A 7	Removed		
A 6	Installed		
I 9	Removed	}	Strapped for Vector Interrupt 300
I 8	Removed		
I 7	Installed		
I 6	Installed		
CON	Removed		Enables Console at Address 777560-777566
HALT	Removed		No action on framing error or break key
PE	Installed 8 places		Parity enabled
1S	Installed 8 places		One stop bit
7B	Installed 8 places		7 data bits
OP	Removed		Even parity

Table 13-1. TMI 8S Communication Configuration - Serial I/O (Cont'd)

Baud Rate Selection			
Channel 1	Input - primary (next proc.) Output - primary broadcast	4800 baud	RS232
Channel 2	Input - primary (prev. proc.) Output - no connection	4800 baud	RS232
Channel 3	Input - secondary (next proc.) Output - secondary broadcast	4800 baud	RS232
Channel 4	Input - secondary (prev. proc.) Output - no connection	4800 baud	RS232
Channel 5	Input - TSX-NET Output - TSX-NET	4800 baud	RS232
Channel 6	Input - Line Printer Output - Line Printer	9600 baud	RS232
Channel 7	Input - Prog. Workstation Output - Prog. Workstation	9600 baud	RS232
Channel 8	Input - Reserved (Non-console) Output - Reserved (Non-console)	300 baud	RS232

Note: Channels 1-8 are numbered SO-S7 on the TMI-8S

Table 13-2. TMI 8S Keyboard I/O Configuration

Address Bits							Address	Keyboard Inputs
A12	A11	A10	A9	A8	A7	A6		
I	I	R	I	R	R	R	*75000	1-8
I	I	R	I	R	R	I	*75100	9-16
I	I	R	I	R	I	R	*75200	17-64
I	I	R	I	R	I	I	*75300	25-32
I	I	R	I	I	R	R	*75400	33-40
I	I	R	I	I	R	I	*75500	41-48
I	I	R	I	I	I	R	*75600	49-56
I	I	R	I	I	I	I	*75700	57-64

Bank (BBS7 L Asserted)

Vector Bits				Address	Keyboard Inputs
9	8	7	6		
R	I	R	R	400	1-8
R	I	R	I	500	9-16
R	I	I	R	600	17-24
R	I	I	I	700	25-32
I	R	R	R	1000	33-40
I	R	R	I	1100	41-48
I	R	I	R	1200	49-56
I	R	I	I	1300	57-64

Table 13-2. TMI 8S Keyboard I/O Configuration (Cont'd)

Channels 1 through 8

Baud Rate: 4800

Protocol: RS 422

Miscellaneous Jumpers

Console	Installed	Disabled console mode on channel 8
Halt	Removed	No action on framing error or break key
PE	Removed (8 places)	Parity disabled
1S	Installed (8 places)	Enable one stop bit
7B	Removed (8 places)	8 data bits
OP	Removed (8 places)	Even parity

13.5 TEST PROCEDURE FOR COMMUNICATIONS 8S INTERFACE.

1. Verify that System power switch is in ON position.
2. Set Electronics Chassis power switch to OFF.
3. Remove MADTS system cable 401-37755-01, P1, P2, and P3 from MADTS system 8S CCA in Electronics Chassis card cage slot A1-L3.
4. Remove MADTS system 8S CCA from slot A1-L3.
5. Insert standard DEC extender board into slot A1-L3. Ensure that extender board is oriented correctly with respect to its key.
6. Insert 8S CCA under test into board extender.
7. Insert MADTS Test Cable 401-37863-01 into Channels 1-4 on 8S CCA under test. See Figure 13-2.
8. Insert MADTS Test Cable 401-37864-01 into Channels 5-7 on 8S CCA under test. See Figure 13-2.
9. Insert MADTS system cable 401-37755-01, P3 into Channel 8 on 8S CCA under test. See Figure 13-2.
10. Set Electronics Chassis Power switch to ON. MADTS will auto boot and prompt operator with following typical message:

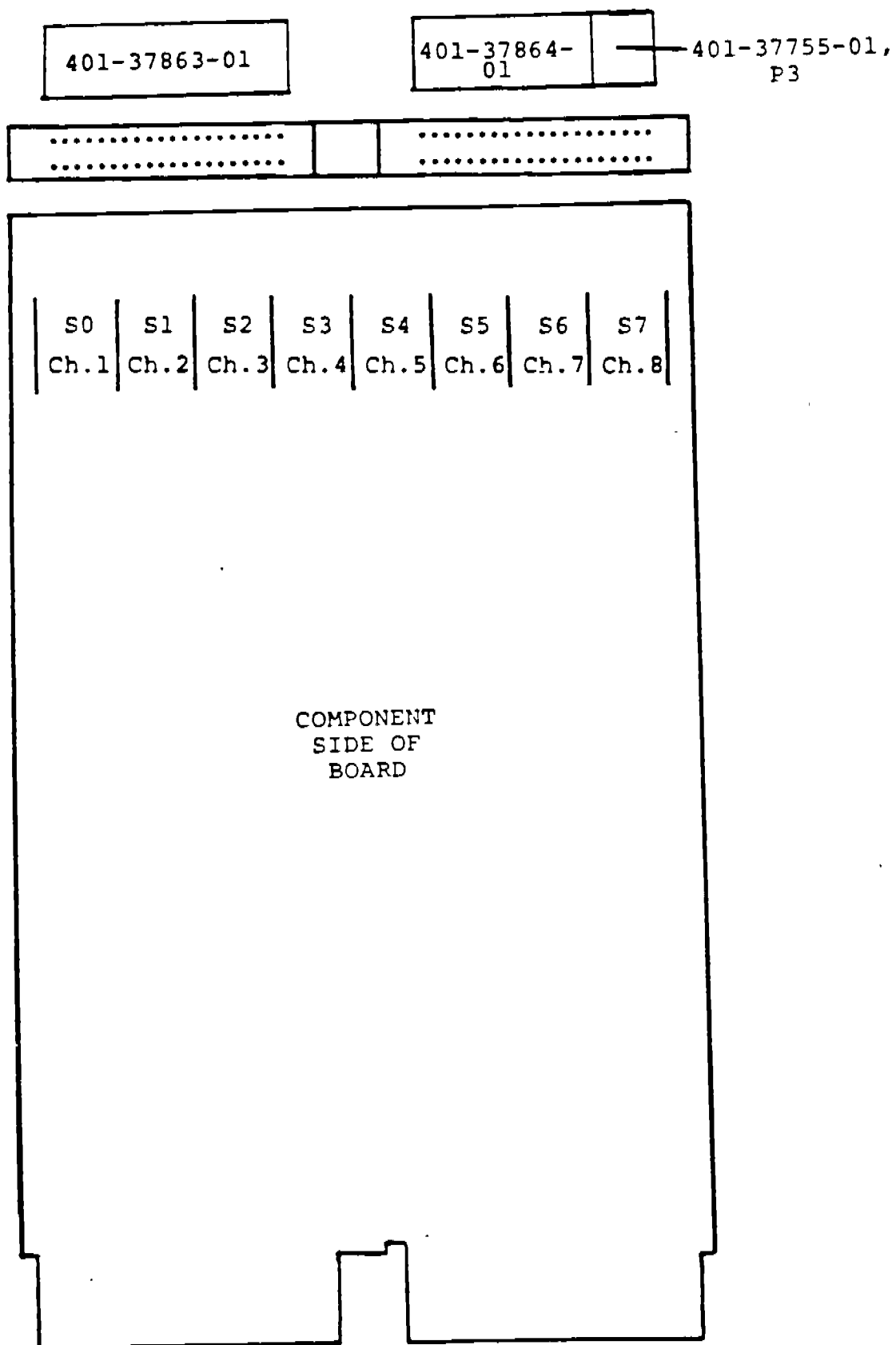


Figure 13-2. 8S Channel Identification

2.

@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....
```

```
0.....1.....2.....3.....4.....5.....6...
0123456789012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****...
RL              *???....
```

```
0.....1.....2.....3.....4.....5.....6...
0123456789012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

11. Input: D DL (CR)

Printer response:

DLDIAG:

12. Input: S SU=16+EU=22 (CR)

Printer response:

DLDIAG:

13. Input: X (CR)

Printer response:

X.

16[BUS	DTR	SWE	SWD	OVR]
17[BUS	DTR	SWE	SWD	OVR]
18[BUS	DTR	SWE	SWD	OVR]
19[BUS	DTR	SWE	SWD	OVR]
20[BUS	DTR	SWE	SWD	OVR]
21[BUS	DTR	SWE	SWD	OVR]
22[BUS	DTR	SWE	SWD	OVR]

DLDIAG:

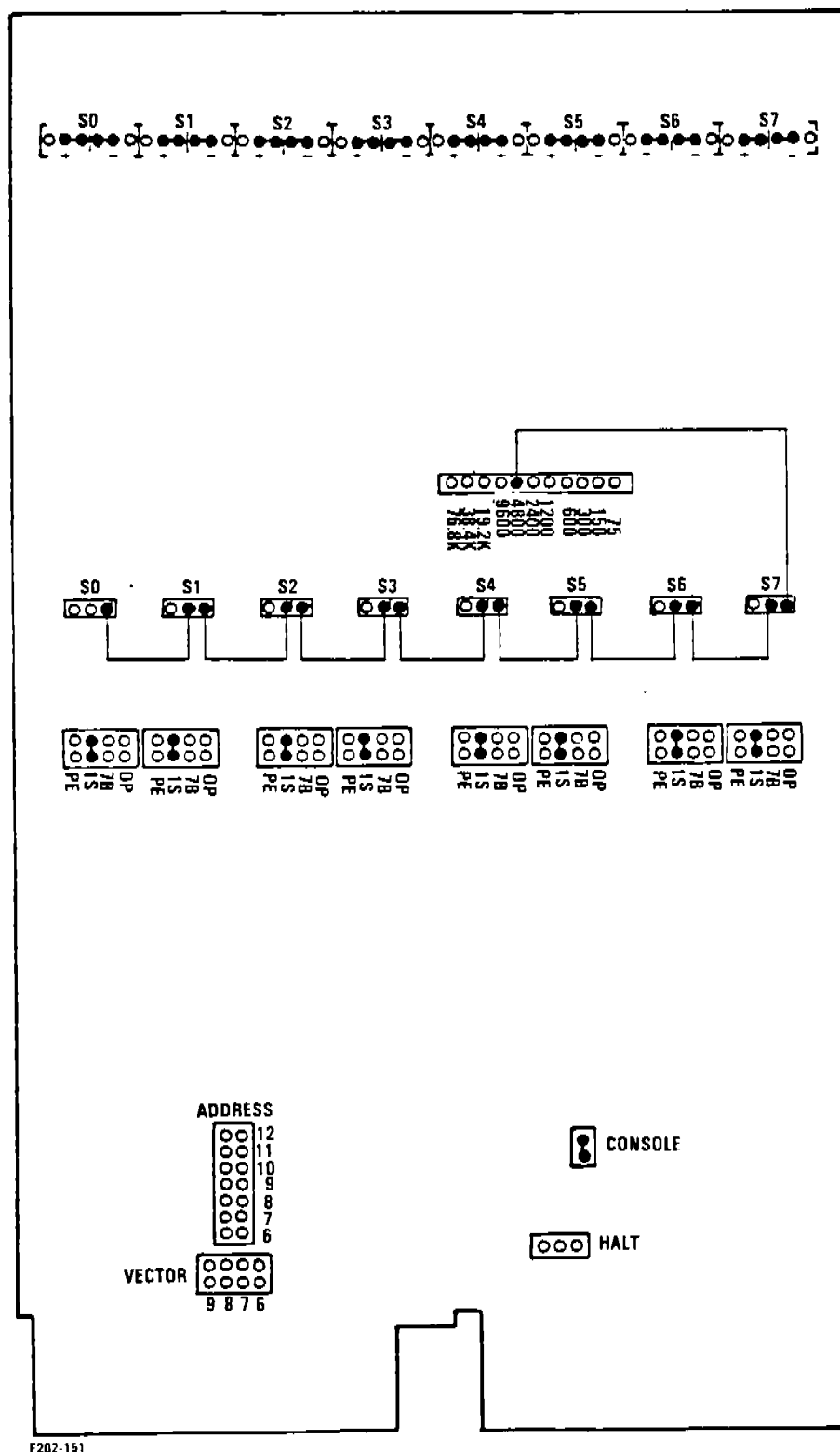
14. The 8S Serial Interface CCA diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.

15. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 13.8 and Table 13-3, 8S Interface Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the 8S Eight Channel Serial Interface Instruction Book (TI 6490.9) for theory of operation and diagrams. Use accepted practices in isolation of faulty component(s).

4S
S SU=16+EU=22

13.6 TEST PROCEDURE FOR KEYBOARD 8S INTERFACE.

1. Verify that 8S CCA has CONSOLE jumper installed (see Figure 13-3) and is jumpered for Channels 1-8 or is jumpered for Channels 9-16. Refer to Table 13-2.
2. Verify that the System Power switch is in ON position.
3. Set Electronics Chassis power switch to OFF.
4. Insert standard DEC extender board into slot A3-L1 in Electronics Chassis card cage. Ensure that extender board is oriented correctly with respect to its key.
5. Insert 8S CCA (unit under test) into the board extender.
6. Insert MADTS Test Cable 401-37863-01 into Channels 1-4 on 8S CCA under test. See Figure 13-4.
7. Insert MADTS Test Cable 401-37863-01 into Channels 5-8 on 8S CCA under test. See Figure 13-4.
8. Set Electronics Chassis Power switch to ON. MADTS will auto boot and prompt operator with following typical message:



F202-151

Figure 13-3. 8S Keyboard Configuration

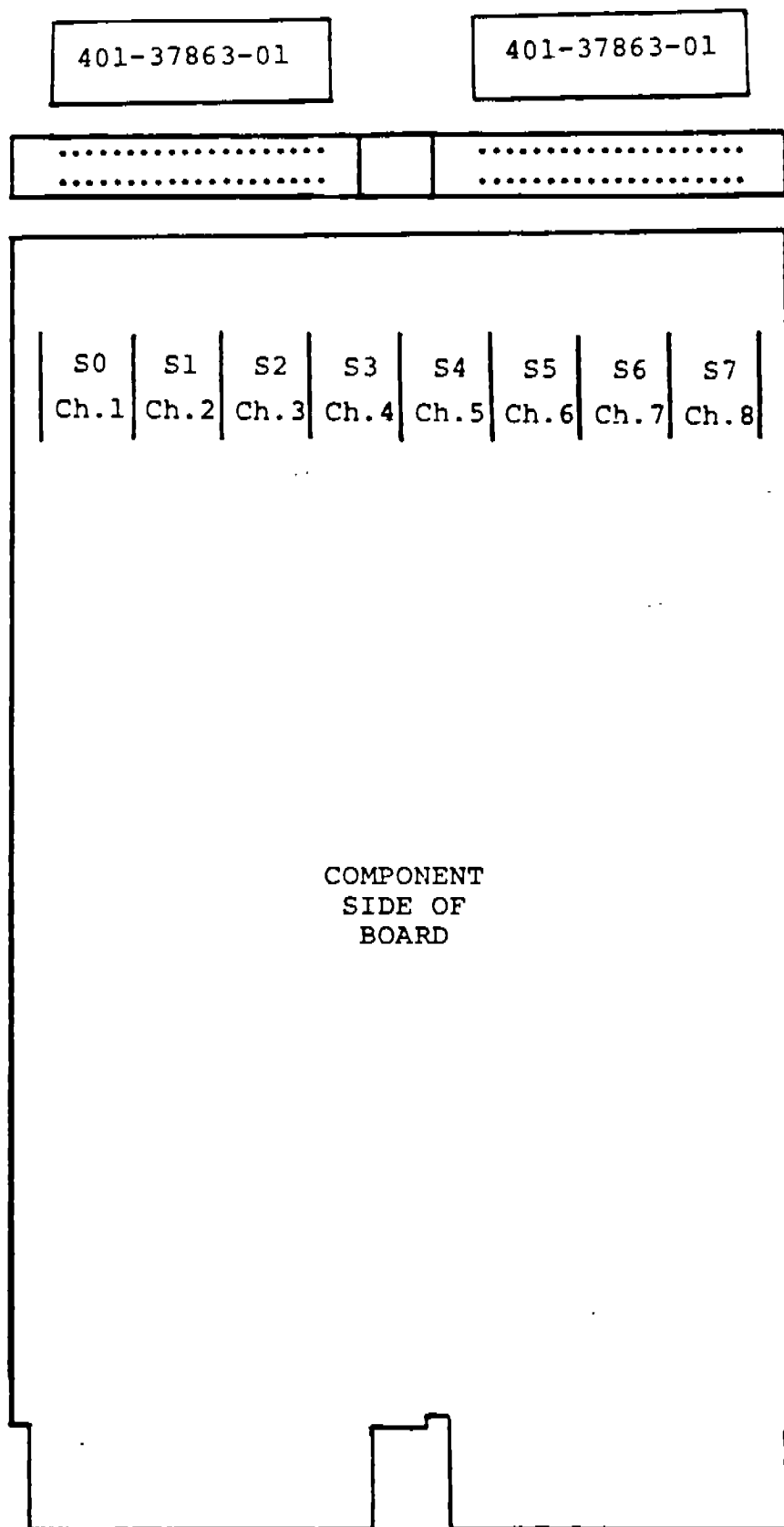


Figure 13-4. 8S Channel Identification

3.
@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

9. Input: D DL (CR)

Printer response:

DL :

10. Input: P DIAG (CR)

Printer response:

DLDIAG:

11. Input: S *

Printer response:

DLDIAG:

12. If 8S CCA under test is jumpered for Channels 1-8 as determined in step 1, input S EU=7 (CR). If 8S CCA is jumpered for Channels 9-16 then input S SU=8+EU=15 (CR).

Printer response:

DLDIAG:

Input: X (CR)

Printer response for Channels 1-8:

```
00[ BUS DTR SWE SWD OVR DTL SEL SDL ]
01[ BUS DTR SWE SWD OVR DTL SEL SDL ]
02[ BUS DTR SWE SWD OVR DTL SEL SDL ]
03[ BUS DTR SWE SWD OVR DTL SEL SDL ]
04[ BUS DTR SWE SWD OVR DTL SEL SDL ]
05[ BUS DTR SWE SWD OVR DTL SEL SDL ]
06[ BUS DTR SWE SWD OVR DTL SEL SDL ]
07[ BUS DTR SWE SWD OVR DTL SEL SDL ]
```

DLDIAG:

Printer response for Channels 9-16:

```
08[ BUS DTR SWE SWD OVR DTL SEL SDL ]
09[ BUS DTR SWE SWD OVR DTL SEL SDL ]
10[ BUS DTR SWE SWD OVR DTL SEL SDL ]
11[ BUS DTR SWE SWD OVR DTL SEL SDL ]
12[ BUS DTR SWE SWD OVR DTL SEL SDL ]
13[ BUS DTR SWE SWD OVR DTL SEL SDL ]
14[ BUS DTR SWE SWD OVR DTL SEL SDL ]
15[ BUS DTR SWE SWD OVR DTL SEL SDL ]
```

DLDIAG:

13. The 8S Keyboard Interface diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.
14. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 13.8 and Table 13-3, 8S Interface Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the 8S Eight Channel Serial Interface Instruction Book TI 6490.9 for theory of operation and diagrams. Use accepted practices in isolation of faulty component(s).

13.7 POWER DOWN SEQUENCE

13.7.1 Power Down Sequence for Communications 8S.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove all cables from 8S CCA under test.
4. Remove 8S CCA from DEC extender board in Electronics Chassis card cage.
5. If additional 8S CCA Communications configurations are to be tested return to paragraph 13.5 step 6 and proceed.
6. Remove DEC extender board from slot A1-L3 in Electronics Chassis card cage.
7. Install MADTS system 8S CCA into slot A1-L3.
8. Insert MADTS system cable 401-37755, P1, P2, and P3 into MADTS system 8S CCA.

13.7.2 Power Down Sequence for Keyboard 8S.

Upon test completion follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove all cables from 8S CCA under test.
4. Remove 8S CCA from DEC extender board in Electronics Chassis card cage.

5. If additional 8S CCA Keyboard configurations are to be tested return to paragraph 13.6 and proceed.
6. Remove DEC extender board from slot A1-L3 in Electronics Chassis card cage.
7. Install MADTS system 8S CCA into slot A1-L3.
8. Insert MADTS system cable 401-37755, P1, P2, and P3 into MADTS system 8S CCA.

13.8 MADTS TMI-8S SERIAL INTERFACE DIAGNOSTIC PROGRAM.

13.8.1 Function Mnemonics. The test function mnemonics used by the TMI-8S serial interface diagnostic program are listed below. Unless otherwise noted, functions are enabled by default for the manual test mode and disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. BUS	Ensures that the four CSRs for the channel under test can be read. Enabled during the automatic test phase.
b. DTR	Tests for cross-talk between seven data transmit and receive lines by transmitting values which cause a single data line to be high with the remaining lines low. Interrupts are enabled.
c. SWE	Tests receive and transmit operation with 7 bit data which emulate a square wave. Interrupts are enabled.
d. SWD	Tests receive and transmit operation with 7 bit data which emulate a square wave. Interrupts are disabled.
e. OVR	Ensures that a read overrun is correctly detected.
f. DTL	Tests for cross-talk between eight data transmit and receive lines with interrupts enabled. This function is disabled by default.
g. SEL	Tests receive and transmit operation with 8 bit data which emulate a square wave. Interrupts are enabled. This function disabled by default.
h. SDL	Tests receive and transmit operation with 8 bit data which emulate a square wave. Interrupts are disabled. This function is disabled by default.

The number of output parameters vary from zero to two depending on the error. The error codes used by the MADTS TMI 8S serial interface diagnostic program and their associated output parameters are given in Table 13-3.

13.8.2 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 13-3. The address and contents of a CSR are normally given in the BFD format. This diagnostic requires that channel under test have a loopback connector attached.

13.8.3 Error Output. Error codes and any associated data are output in the following form:

```
ERROR #xxxx      aaaaaa  bbbbbb
```

where:

```
xxxx   is the error number
aaaaaa is the first output parameter
bbbbbb is the second output parameter
```

The TMI-8S has eight asynchronous serial I/O channels and is compatible with the DEC DRV11-J. Four CSR registers are associated with each channel: two for input and two for output. The following CSR assignments are useful for troubleshooting. The assignments for each test mode are shown.

CSR for serial read control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	A	B	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

A - receive interrupt enable
B - done

CSR for serial read

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	E	E	E	E	E	E	E
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

A - input error
B - overrun error
C - framing error
D - parity error
E - data

CSR for serial write control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	A	B	0	0	0	0	C
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

A - transmit ready
 B - interrupt enable
 C - transmit break

CSR for serial write

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	A	A	A	A	A	A	A
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:

A - data

Table 13-3. 8S Serial Interface Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
BUS	Read CSRs	The four CSRs associated with the port number under test are each read. A non-existent CSR will result in a BUS time-out.	0	A BUS timeout occurred while attempting to read the CSR.	None
DTR	Transmit/Receive test	The values 0, 1, 2, 4, 10, 20, 40, and 100 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a character is transmitted, a transmit interrupt is received, and verified. The transmit ready bit of the TCSR register should be set. A receive interrupt is then received and verified. The receive ready bit of the RCSR register should be set. Finally, the value received is compared to the value transmitted.	2	Transmit CSR bit 7 (transmit ready) did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 (receive ready) did not get set.	CSR contents (BFD)
			10	A transmit interrupt failed to occur.	CSR contents (BFD)
			12	A receive interrupt failed to occur.	CSR contents (BFD)
			14	An incorrect transmit interrupt vector was received.	Interrupt vector received
			16	An incorrect receive interrupt vector was received.	Interrupt vector received.

Table 13-3. 8S Serial Interface Diagnostic Error Message Description
(Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DTR (Cont.)			18	The character received does not match the character transmitted.	CSR contents (BFD) Expected character Actual character
SWE	Transmit/Receive test	The values 125 and 052 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a value is transmitted, a transmit interrupt is received and verified. The transmit ready bit of the TCSR register should be set. A receive interrupt is then received and verified. The receive bit of the RCSR register should be set. Finally, the value received is compared to the value transmitted.	2	Transmit CSR bit 7 (transmit ready) did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 (receive ready) did not get set.	CSR contents (BFD)
			10	A transmit interrupt failed to occur.	CSR contents (BFD)
			12	A receive interrupt failed to occur.	CSR contents (BFD)
			14	An incorrect transmit interrupt vector was received.	Interrupt vector received
			16	An incorrect receive interrupt vector was received.	Interrupt vector received.

Table 13-3. 8S Serial Interface Diagnostic Error Message Description
(Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SWE (Cont.)			18	The character received does not match the character transmitted.	CSR contents (BFD) Expected character Actual character
SWD	Transmit/Receive test	The values 125 and 052 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a value is transmitted, a transmit interrupt should not occur. The transmit ready bit of the TCSR register should be set. The receive ready bit of the RCSR register should also be set. Finally, the value received is compared to the value transmitted.	2	Transmit CSR bit 7 did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 did not get set.	CSR contents (BFD)
			6	A transmit interrupt occurred with the transmit interrupts disabled.	CSR contents (BFD)
			18	The character received does not match the character which was transmitted.	CSR contents (BFD) Expected character Actual character
OVR	Receive overrun test	Interrupts are disabled. A 0 is transmitted via the TBUF register and looped back to the RBUF register. A transmit	6	A transmit interrupt occurred with transmit interrupts disabled.	CSR contents (BFD)

Table 13-3. 8S Serial Interface Diagnostic Error Message Description
(Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
OVR (Cont.)		interrupt is received. A second 0 is transmitted without first reading RBUF. The receive error bit (15) of RBUF is checked to verify that a receive error was detected. Bit #14 is then checked to verify that a receive overrun error was detected.	20	The receive overrun error bit did not get set when a receive overrun was induced.	CSR contents (BFD)
			22	The receive error bit did not get set when a receive overrun was induced.	CSR contents (BFD)
DTL	Transmit/Receive test	The values 0, 1, 2, 4, 10, 20, 40, 100, and 200 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a character is transmitted, a transmit interrupt is received and verified. The transmit ready bit of the TCSR register should be set. A receive interrupt is then received and verified. The receive ready bit of the RCSR register should be set. Finally, the values	2	Transmit CSR bit 7 (transmit ready) did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 (receive ready) did not get set.	CSR contents (BFD)
			10	A transmit interrupt failed to occur.	CSR contents (BFD)
			12	A receive interrupt failed to occur.	CSR contents (BFD)
			14	An incorrect transmit interrupt vector was received.	Interrupt vector received

Table 13-3. 8S Serial Interface Diagnostic Error Message Description
(Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DTL (Cont.)		received is compared to the value transmitted.	16	An incorrect receive interrupt vector was received.	Interrupt vector received
			18	Value received does not match the value that was transmitted.	CSR contents (BFD) Expected value Actual value
SEL	Transmit/Receive test	The values 125 and 252 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a value is transmitted, a transmit interrupt is received and verified. The transmit ready bit of the TCSR should be set. A receive interrupt is then received and verified. The receive ready bit of the RCSR should be set. Finally, the value received is compared to the value transmitted.	2	Transmit CSR bit 7 (transmit ready) did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 (receive ready) did not get set.	CSR contents (BFD)
			10	A transmit interrupt failed to occur.	CSR contents (BFD)
			12	A receive interrupt failed to occur.	CSR contents (BFD)
			14	An incorrect transmit interrupt vector was received.	Interrupt vector received
			16	An incorrect receive interrupt vector was received.	Interrupt vector received

Table 13-3. 8S Serial Interface Diagnostic Error Message Description
(Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SEL (Cont.)			18	The character received does not match the character which was transmitted.	CSR contents (BFD) Expected value Actual value
SDL	Transmit/Receive test	The value 125 and 252 (octal) are transmitted via the TBUF register and looped back to the RBUF register. After a value is transmitted a transmit interrupt should not occur. The transmit ready bit of the TCSR should be set. The receive ready bit of the RCSR should also be set. Finally, the value received is compared to the value transmitted.	2	Transmit CSR bit 7 (transmit ready) did not get set.	CSR contents (BFD)
			4	Receive CSR bit 7 (receive ready) did not get set.	CSR contents (BFD)
			6	A transmit interrupt occurred with transmit interrupts disabled.	CSR contents (BFD)
			18	The character received does not match the character which was transmitted.	CSR contents (BFD) Expected character Actual character

SECTION XIV
LRU TEST PROCEDURES
KPV11-B ASSEMBLY

14.1 GENERAL. This section contains the test procedures for the KPV11-B assembly as tested on the MADTS. The test is conducted under diagnostic software control, and has several functions which are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

14.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the KPV11-B:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
Standard Dual Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test.

14.3 OTHER DOCUMENTATION. The only other documentation required for test is the KPV11-B Instruction Manual (TI 6490.5).

14.4 PREPARATION FOR TEST. To prepare the KPV11-B for test, follow the instructions listed below.

1. Verify that System POWER switch is set to ON position.
2. Set Electronics Chassis Power Switch to OFF position.
3. Lift MADTS system KPV11-B card out of slot A3-L4 enough to allow removal of black, green, and white wires.
4. Disconnect black, green, and white wires (P/N 401-37295) from MADTS system KPV11-B board in slot A3-L4 in card cage of Electronics Chassis. Note placement of these wires.
5. Remove MADTS system KPV11-B in card slot A3-L4.
6. Insert standard DEC dual board extender into slot A3-L4 in card cage of Electronics Chassis so that board extender is oriented correctly with respect to its key.
7. Insert KPV11-B (unit under test) into extender board, so that KPV11-B is oriented correctly with respect to its key.

8. Reconnect wires (P/N 401-37295) in same order as they were on board which was in machine -- i.e., black wire is closest to back of machine, followed by green wire, and the white wire.

14.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

2-
@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???.

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-115J (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****...
RL              *???.
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D KP (CR)

Printer response:

KPDIAG:

2. Input: X (CR)

Printer response:

00 [BUS BIT CKD CKE INT TIM]

KPDIAG:

3. The KPV11-B diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.
4. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 14.7 and Table 14-1, KPV11-B Diagnostic Error Message Description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the KPV11-B Instruction Book (TI 6490.5) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty components.

14.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove all cables from KPV11-B board.
4. Remove KPV11-B from extender board.
5. If additional KPV11-B boards are to be tested, return to paragraph 14-4, step 6, and proceed.
6. Remove extender board from card slot A3-L4.

7. Reconnect cable P/N 401-37295 to MADTS system KPV11-B. Refer to paragraph 14-4, step 8.
8. Replace MADTS system KPB11-B into card slot A3-L4 in Electronics Chassis card cage.

14.7 MADTS KPV11-B LINE TIME CLOCK DIAGNOSTIC PROGRAM.

TYPE: SYS MOD

I.D.: SYSTEM MODULE

PART NUMBER: KPV11-B

CONFIGURE PER SPEC: 406-02153

14.7.1 Calling Sequence.

14.7.2 Function Mnemonics.

The test function mnemonics used by the Line Time Clock diagnostic program are as follows. Unless other noted, functions are enabled by default for the manual test mode and disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. BUS	Ensures that the KPV11-B CSR can be read from and written to. Enabled during the automatic test phase.
b. BIT	Ensures that setting all the CSR bits does not set bits 0 through 5 or bits 8 through 15. Enabled during the automatic test phase.
c. CKD	Ensures that CSR bit 7 gets set after enough time has elapsed for at least one tick to have occurred. Interrupts are disabled. Interrupts are enabled during the automatic test phase.
d. CKE	Ensures that CSR bit 7 gets set after enough time has elapsed for at least one tick to have occurred. Interrupts are enabled. Enabled during the automatic test phase.
e. INT	Ensures that clock interrupts occur when enabled and do not occur when disabled. Enabled during the automatic test phase.
f. TIM	Ensures that a clock tick is of the proper duration.

14.7.3 Function Stimuli Descriptions.

A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 14-1. The address and contents of a CSR is normally given in the BFD format.

14.7.4 Error Output.

Error codes and any associated data is output in the following form:

```
ERROR #xxxx    aaaaaa    bbbbbb
```

where:

```
xxxx    is the error number
aaaaaa  is the first output parameter
bbbbbb  is the second output parameter
```

The number of output parameters varies from zero to two depending on the error. The error codes used by the MADTS KPV11-B diagnostic program and their associated output parameters are given in Table 14-1.

Table 14-1. KPV11-B Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
BUS	Read CSR	The KPV11-B CSR is read.	0	A bus time-out occurred while attempting to read the CSR.	none
BIT	Test CSR bits	All ones are written to the CSR. Bits 6 and 7 are cleared. The CSR is then read for verification.	10	Was able to set one or more bits in the range 0-5 and 8-15.	CSR contents (BFD)
CKD	Clock transition	CSR bits 6 and 7 are cleared. After approximately 1 "tick" interval has elapsed, bit 7 is tested to verify that it was set.	12	CSR bit 7 was not set within the 1/60 second time allowed.	CSR contents (BFD)
CKE	Clock	CSR bit 7 is cleared. Bit 6 is set to enable interrupts. After approximately 1 "tick" interval has elapsed, bit 7 is tested to verify that it was set.	12	CSR bit 7 was not set within the 1/60 second time allowed.	CSR contents (BFD)
INT	Interrupt Enable Test	CSR bit 7 is cleared and interrupts are enabled. An interval of 1 "tick" is given for an interrupt to occur. The interrupt vector is verified. Bit 7 is then checked to ensure that it was set.	12	CSR bit 7 was not set within the 1/60 second time allowed.	CSR contents (BFD)
			16	An interrupt did not occur within 1/60 second after interrupts were enabled.	CSR contents (BFD)

Table 14-1. KPV11-B Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
INT	Inter- rupt disable test	CSR bit 7 is cleared and interrupts are disabled. An interval of 1 "tick" is given for an interrupt to occur, and bit 7 is checked to ensure that it was set. The bit is then cleared.	20	An interrupt vector other than 100 was received.	The interrupt vector that was received
			8	Could not clear bit 7.	CSR contents (BFD)
			12	CSR bit 7 was not set within the 1/60 second time allowed.	CSR contents (BFD)
			14	An interrupt occurred with interrupts disabled.	CSR contents (BFD)
TIM	Clock timing test	CSR bit 7 is cleared and interrupts are disabled. Bit 7 is repeatedly checked for approximately 1 second. Each time the bit is set, an internal counter is incremented and the bit is cleared. At the end of the 1 second interval the value of the counter is checked. The value should be 60 (60 ticks per second), with an error tolerance of 5 ticks for CPU loop timing.	18	The correct number of ticks were not generated by the clock during approximately 1 second (60 ticks) of CPU time.	# clock ticks required # clock ticks expected

SECTION XV
LRU TEST PROCEDURES
PRINTRONIX LINE PRINTER

15.1 GENERAL. This section contains the test procedures for the Printronix Line Printer, Model P300, as tested on the MADTS. The test is conducted under diagnostic software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

15.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for testing the Printronix Line Printer:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
MADTS Test Cable	E-Systems P/N 401-37126-17

Tools other than standard shop tools are not required in test of the Printronix Line Printer.

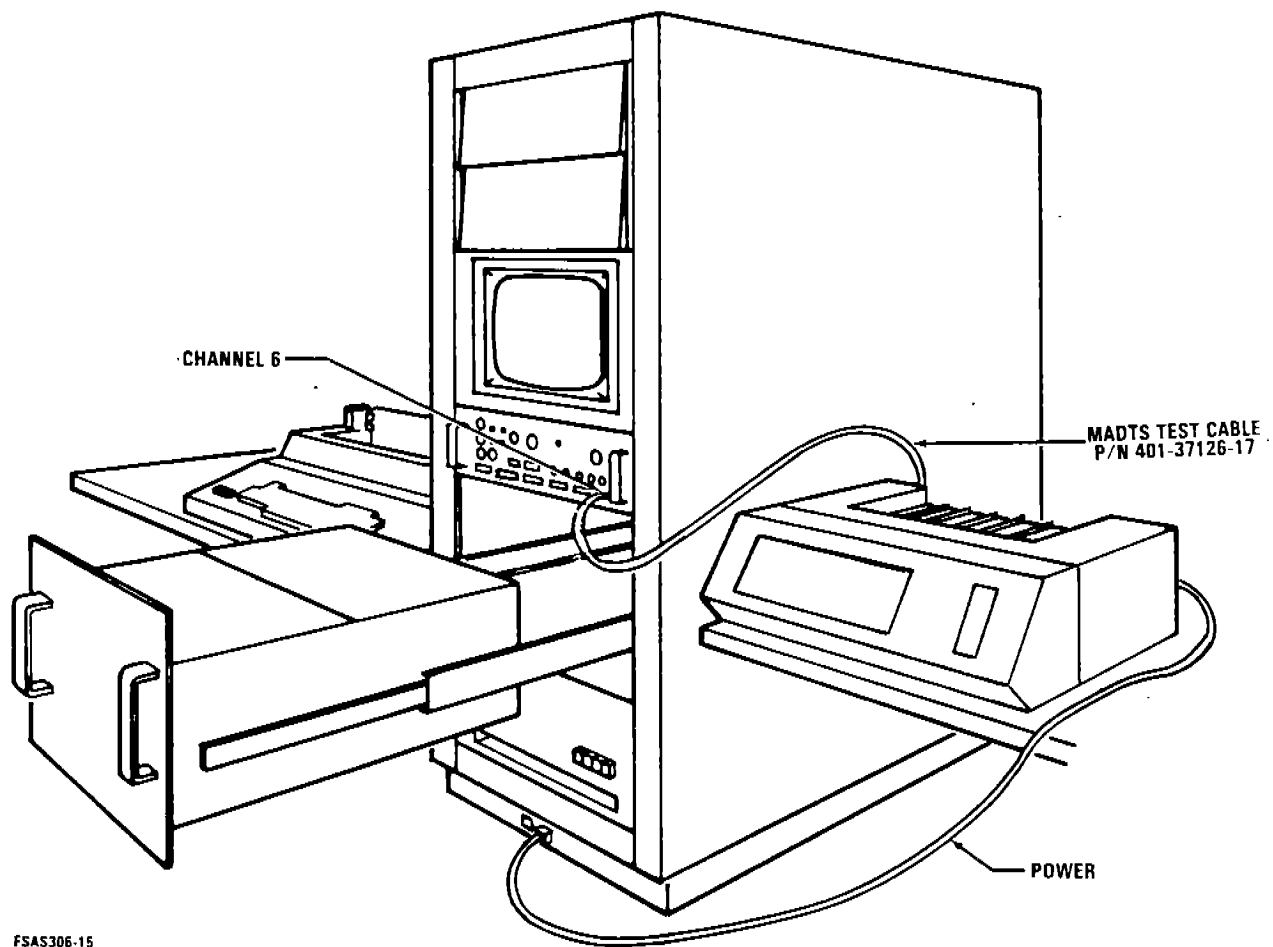
15.3 OTHER DOCUMENTATION. Other documentation required for test of the Printronix Line Printer is listed below.

Instruction Manual, P300 Line Printer, Volumes I, II, and III, (TI 6490.13)

15.4 PREPARATION FOR TEST. To prepare the Printronix P300 Line Printer for test, follow the instructions listed below. The test set-up for the printer is shown in Figure 15-1.

1. Verify that P300 Line Printer is configured as in Tables 15-1, 15-2, and 15-3. Also see Figures 15-2, 15-3, and 15-4.
2. Verify that System Power switch is set to ON position.
3. Set Electronics Chassis Power switch to OFF.
4. Connect MADTS test cable 401-37126-17, P1, to Channel 6 on the I/O Control Panel.
5. Connect MADTS test cable 401-37126-17, P2, to RS-232 port on Printronix P300 Line Printer.
6. Set Printronix P300 Line Printer Power switch to ON and press ON-LINE button (the light will come on when it is ON-LINE).

15.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:



FSAS306-15

Figure 15-1. Printronix Line Printer Set-Up

Table 15-1. Jumper Configuration for RS-232 Board

HYBRID CURRENT LOOP DISABLE - Installed		
CURRENT LOOP ENABLE - Removed		
DSR		- Removed
ACK/NACK PROG. RECD.		
	CHARACTER	- Removed
BIT 8		
	P1 to GND	- Installed
	DATA to GND	- Installed
CURRENT LOOP OUT		
	A (both places)	- Installed
REQ TO SEND		
	AFSS	BSY - Installed, NBSY - Removed
	FSDPS	NBSY - Installed, BSY - Removed
DRT		
	<u>BSY</u>	- Installed
DATA TRANSMIT		
	TOB	- Installed
REVERSE CHANNEL		
	NBSY	- Installed
BAUD RATE		
	9.6K	- Installed

Table 15-1. Jumper Configuration for RS-232 Board (Continued)

CURRENT LOOP OUT

TOB - Installed

2K BUFF - Removed

ODD PARITY

PAR ENAB	-	Installed
128	-	Installed
512	-	Installed

BAFL

HYS - Installed

DIS PAR ERR - Removed

2K BUF - Removed

1024 BAFL - Removed

ON-ACK	8	Installed
	1	Removed
	7	Installed
	2	Installed
	6	Installed
	3	Installed
	5	Removed
	4	Installed

OFF-NACK

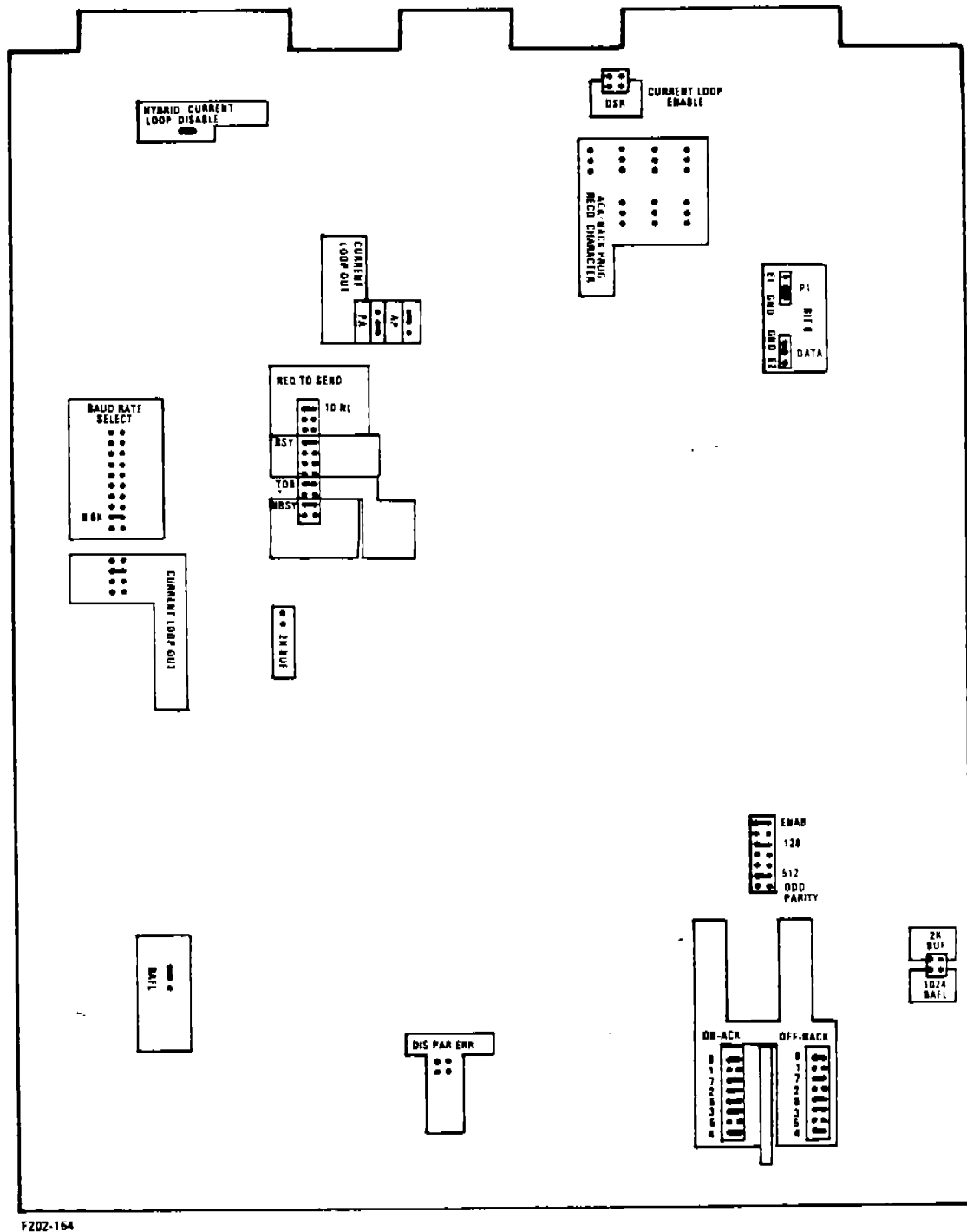
8	Installed
1	Removed
7	Installed
2	Removed
6	Installed
3	Installed
5	Removed
4	Installed

Table 15-2. Logic A Printed Circuit Board Assembly P300 Line Printer

<u>FUNCTION</u>	<u>JUMPER</u>	<u>PINS</u>	<u>EXPLANATION</u>
Location 8K			
Auto Line Feed	W1	1-14	Omit
Line Feed with Carriage Return	W2	2-13	Omit
Underline	W3	3-12	Omit
Data Line 8	W4	4-11	Connect
VFU Control (PI)	W5	5-10	Connect: PI Line not used
Upper-case Enable	W6	6-9	Connect: Lower-case PROM Removed (ICs F1 and F2)
Polarity Select	W7	7-8	Omit: High-true interface

Table 15-3. Logic B Printed Circuit Board Assembly P300 Line Printer

<u>FUNCTION</u>	<u>JUMPER</u>	<u>PINS</u>	<u>EXPLANATION</u>
Location 8K			
Skip-area perforation	W1	1-14	Omit
	W2	2-13	Omit
	W3	3-12	Connect: Sets skip-over distance
Plotting Speed	W4	4-11	Omit: Disable double speed plotting at lower densities
(Not assigned)	W5	5-10	Omit
Paper motion detector	W6	6-9	Connect: Factory Installed
VFU Disable	W7	7-8	Omit: Enables all VFU functions
Location 10A			
8LPI/10LPI	W9	2-13	Connect
	W10	3-12	Omit
	W13	6-8	Connect
	W14	7-8	Omit: Enables 8LPI
Skip-over Perforation	W12	5-10	Connect
Location 22.A	W15	A-B	Omit: 8LPI/6LPI
8LPI(10LPI) only			Software Selected
Location 11K			
Paper-out Delay Override	W27		Omit
	W28		Connect: Enable printing of last two inches of last form



F202-154

Figure 15-2. RS-232 P/N 104374-001K Jumper Configuration

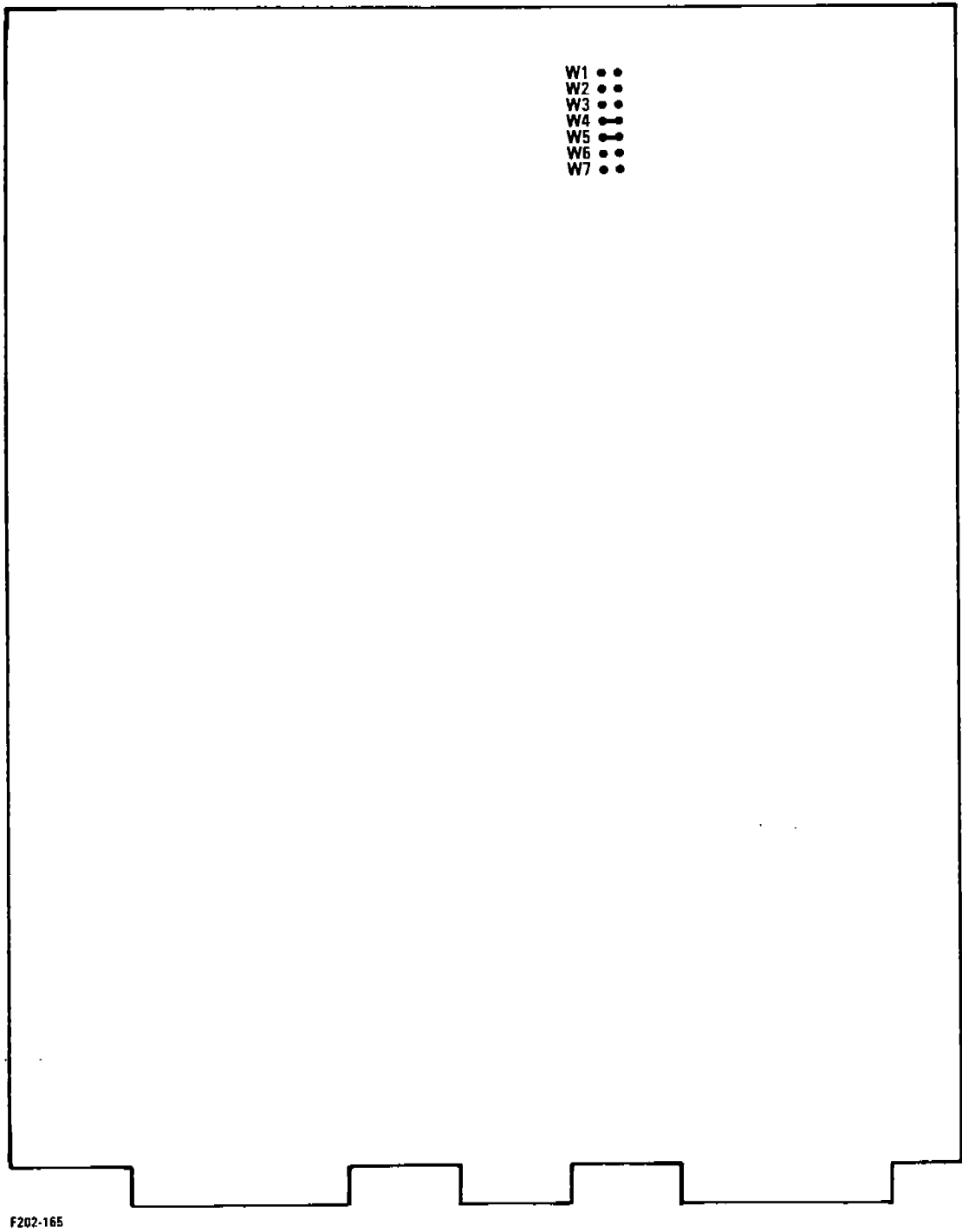


Figure 15-3. Logic A PCBA P/N 101685-001AC Jumper Configuration

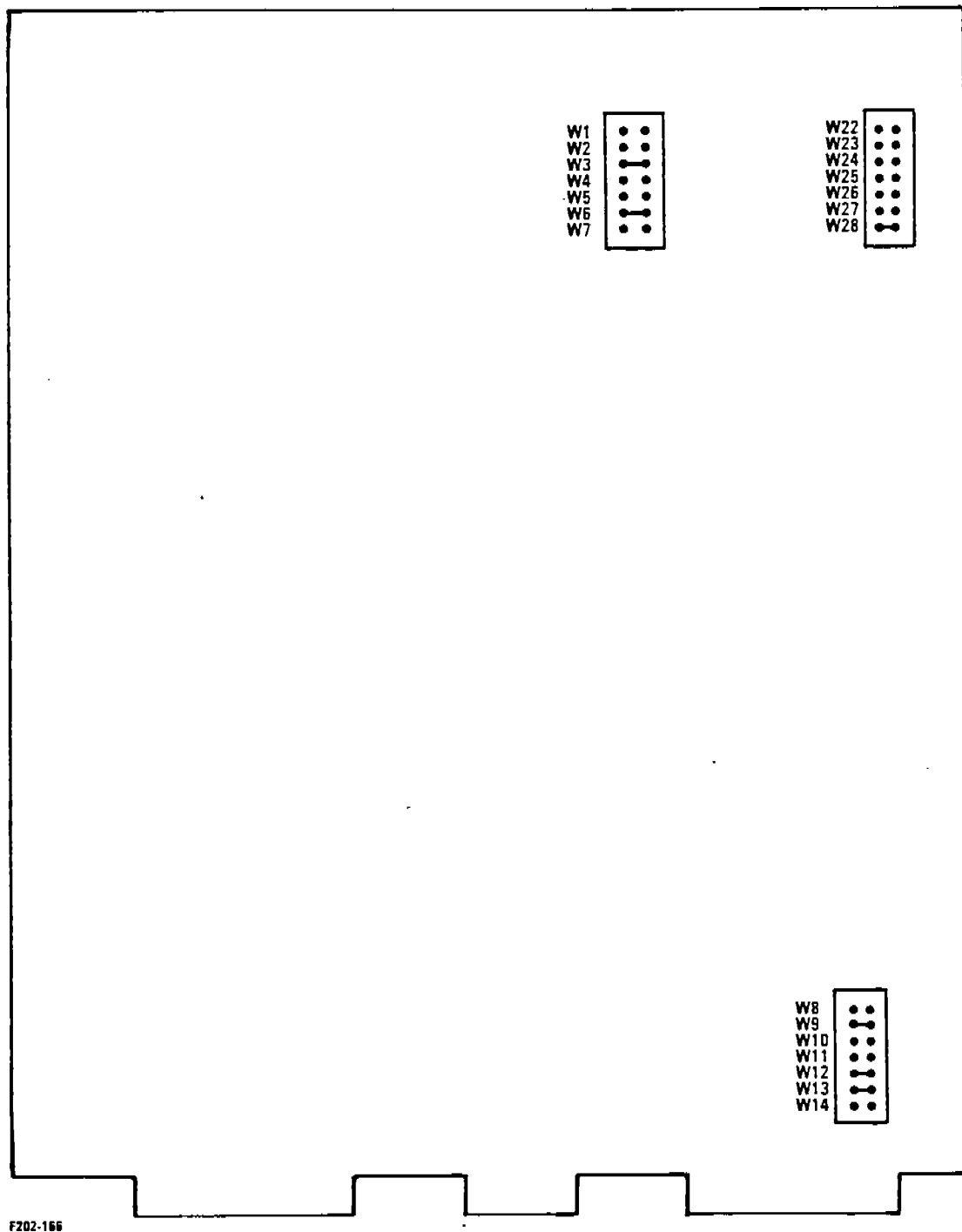


Figure 15-4. Logic B PCBA P/N 102360-001S Jumper Configuration

2.
e

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???.

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ***.....
RL              *???.
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D LP (CR)

Printer response:

LPDIAG:

2. Input: X (CR)

Printer response:

X.

00 [PRI FFT CHR VER HOR WOR HAM ERR

Detach paper from printer then press RETURN to
continue

3. Detach printer paper at the first performance below the Printronix P300 Line Printer.
4. The Printronix P300 Line Printer printout should match the sample shown in Figure 15-5.

5. Input: (CR)

Printer response:

Install printer paper then press RETURN to continue

6. Check to see that CHECK light is ON.
7. Install printer paper in the Printronix P300 Line Printer.
8. Input: (CR)

Printer response:

]

LPDIAG:

9. The Printronix P300 Line Printer diagnostic test is complete. If no errors were reported by MADTS, the unit under test is good.

[illegible]

10. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 15.7 and Table 15-4, printer diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the P300 Line Printer Instruction Book (TI 6490.13) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty components.

15.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set Printronix P300 Line Printer to OFF-LINE by pressing ON-LINE button (the light will go off when it is OFF-LINE), and switch power to OFF.
2. Disconnect MADTS test cable 401-37126-17 (P2) from Printronix Line Printer.
3. If additional Printronix P300 Line Printers are to be tested, return to paragraph 15-4, step 4, and proceed.
4. Set momentary BOOT/HALT switch to HALT position.
5. Set Electronics Chassis Power switch to OFF position.
6. Disconnect MADTS test cable (401-37126-17) (P1) from Channel 6 on I/O Control Panel.

15.7 MADTS PRINTRONIX LINE PRINTER DIAGNOSTIC PROGRAM.

15.7.1 Calling Sequences.

Device: LP
Program: DIAG

15.7.2 Function Mnemonics. The test function mnemonics used by the Printronix Line Printer diagnostic program are as follows. Unless otherwise noted, functions are enabled by default for the manual test mode and are disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. PRI	Sends a line of spaces to the printer to exercise a majority of the print functions without printing.
b. FFT	Allows the user to confirm that the form feed function is operating correctly.
c. CHR	Prints all characters sequentially according to the ASCII sequence.
d. VER	Prints a line of E's to check the vertical dot alignment.
e. HOR	Prints a line of H's to check the horizontal dot alignment.
f. WOR	Prints a line of #'s to print the maximum number of dots in a character.
g. HAM	Exercises all hammers in each of the nine dot-matrix rows and each of the six-dot matrix columns at each character position.
h. ERR	Ensures tht the XON and XOFF characters are properly sent by the printer. It also tests the printer's paper-out detector.

15.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The address and contents of a CSR are normally given in the BFD. The stimuli for each function and associated error data is given in Table 15-4.

15.7.4 Error Output.

Error codes and any associated data are output in the form

ERROR #xxxx

where:

xxxx is the format number

The error codes used by the MADTS Printronix diagnostic program and their associated output parameters are given in Table 15-4.

Table 15-4. Printer Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PRI	Print Line	A line of spaces is sent to the printer. Receipt of an XOFF from the printer will result in the suspension of character transmission until an XON character is received. This should not occur during this test.	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted amount of time.	None
FFT	Form Feed Test	A form feed character is sent to the printer. A "form feed test" message is printed at the top of the following page. Receipt of an XOFF from the printer will result in the suspension of character transmission until, an XON	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial	CSR contents (BFD)

Table 15-4. Printer Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
FFT (cont'd)		character is received. This should not occur during this test.		character from the line printer.	
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted amount of time.	None
CHR	Print Characters	Multiple lines containing each displayable character are sent to the printer. Each line is shifted left one position from the line preceding it. This creates a 'ripple' or 'rolling' pattern. This stimulus will print 7 lines with each pass. A continuous pattern can be generated by enabling the 'loop-on' function of the software. Receipt of an XOFF from the printer will result in the suspension of character trans-	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			8	A framing error occurred during the receipt of a serial character from the line printer.	CSR contents (BFD)

Table 15-4. Printer Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CHR (cont'd)		missions until an XON character is received.	10	An expected XON character was not received within the allotted amount of time.	None
VER	Print Line	A line of E's is sent to the printer. Receipt of an XOFF character from the printer will result in the suspension of character transmission until an XON character is received. This should not occur during this test.	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted amount of time.	None

Table 15-4. Printer Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
HOR	Print Line	A line of H's is sent to the printer. Receipt of an XOFF from the printer will result in the suspension of character transmission until an XON character is received. This should not occur during this test.	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted time.	None
WOR	Print Line	A line of #'s is sent to the printer. Receipt of an XOFF from the printer will result in the suspension of character transmission until an XON character is received. This should not occur during this test.	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial	CSR contents (BFD)

Table 15-4. Printer Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WOR (cont'd)				character from the line printer.	
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted time.	None
HAM	Hammer Test	All hammers in each of the nine dot matrix rows are successively exercised in order to test their horizontal alignment. The same exercise is performed for each of the six matrix columns at each character position. The stimulus is completed by exercising all hammers in all character positions simultaneously. Receipt of an XOFF from the printer will result in the suspension of data transmission until an XON is received.	4	A parity error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the line printer.	CSR contents (BFD)
			10	An expected XON	None

Table 15-4. Printer Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
				Character was not received within the allotted time.	
ERR	XON/XOFF Test	Fills the printer buffer to cause an XOFF to be sent and then confirms that an XON is sent as the buffer empties.	10	An expected XON was not received within the allotted time.	None
			12	An expected XOFF character was not received within the allotted time.	None
	Paper Out Test	The operator is prompted to detach the paper from the printer. Detaching at any perforation between the paper entry point and the paper pack will be sufficient for the test. After a (CR) is typed by the specialist, three form feed characters are sent to the printer in order to exhaust the remaining paper, which should cause an XOFF character to be generated by the printer.	12	An expected XOFF character was not received within the allotted time.	None
	Paper Reload	The operator is prompted to reload the paper and type a (CR) to continue.	None		

SECTION XVI
LRU TEST PROCEDURES
KENNEDY 9000 MAGNETIC TAPE DRIVE

16.1 GENERAL. This section contains test and troubleshooting procedures for the Kennedy 9000 Magnetic Tape Drive, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

16.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the tape drive.

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
MADTS Test Cable	E-Systems P/N 401-37872-01
MADTS Test Cable	E-Systems P/N 401-37846-01
MADTS Test Cable	E-Systems P/N 401-37845-01
TC01 Assembly	Emulex P/N TU0110401
TC01 Assembly	Emulex P/N TU0110406
Scratch Tape	

16.3 OTHER DOCUMENTATION. Refer to the Kennedy 9000 Instruction Book (TI 6490.11) for detailed information on the tape drive.

16.4 PREPARATION FOR TEST. To prepare the tape drive for test, follow the instructions listed below.

1. Verify that System Power Switch is set to ON position.
2. Set Electronics Chassis Power switch to OFF position.
3. Ensure that Emulex TC01 Controller CCA, TU0110401 is in slot A3-1 of the Electronics Chassis card cage and that SW1 is set to 45.0 ips.
4. Ensure that Emulex PE Read CCA, TU1110406 is in slot A3-2 of Electronics Chassis card cage and that SW1 is set to 45.0 ips.
5. Insert MADTS test cable P/N 401-37872-01, P1 into J-1 of Emulex board in slot A3-1 and insert P2 of test cable into J-1 of Emulex board in slot A3-2.
6. Insert MADTS test cable P/N 401-37845-01, P1 into J-2 of Emulex board in slot A3-1.

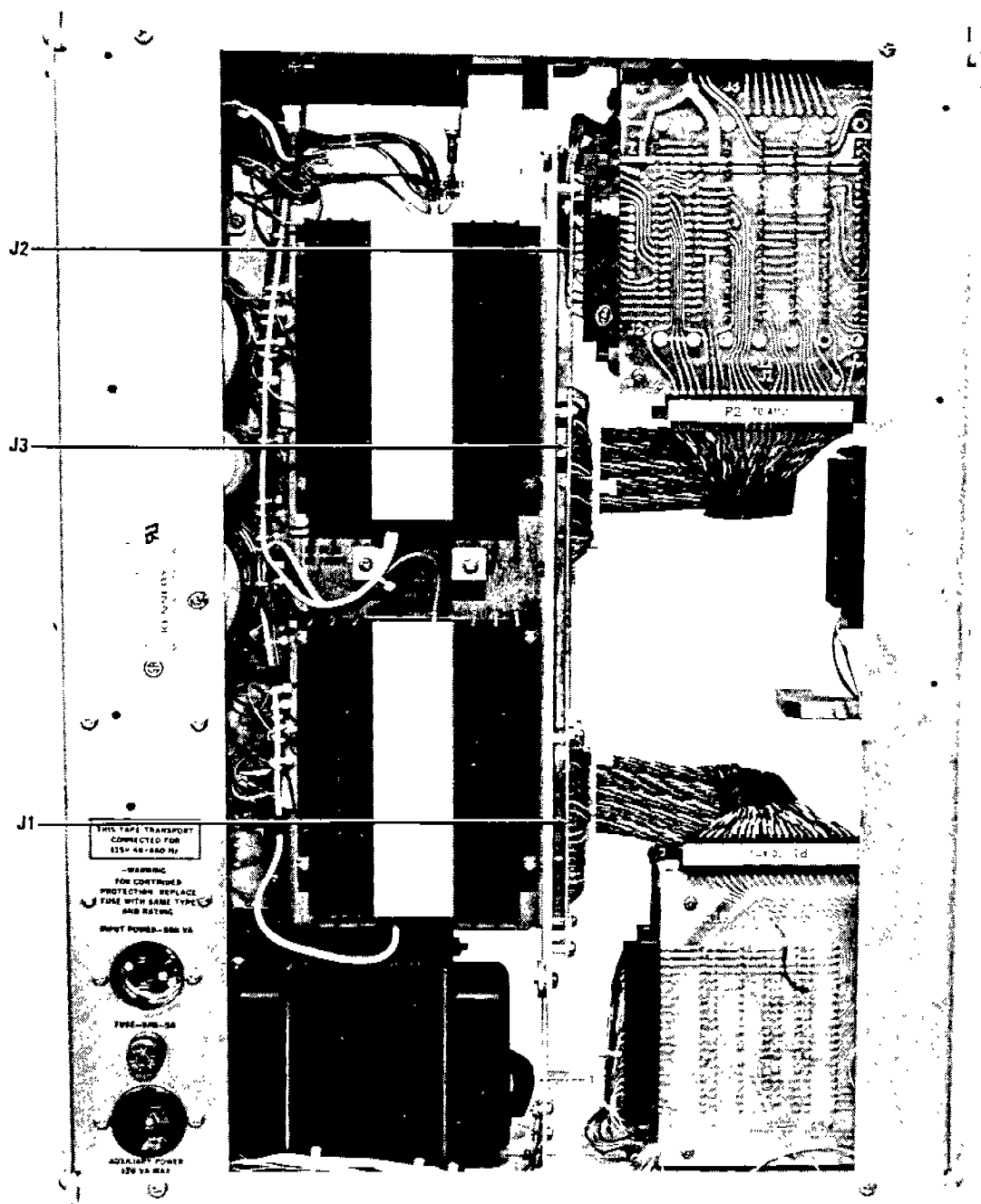
7. Insert MADTS test cable P/N 401-37846-01, P1 into J-2 of Emulex board in slot A3-2.
8. Insert MADTS test cable P/N 401-37846-01, P2 into top board edge connector J2 and P3 into middle board edge connector J3 in back of tape drive. See Figure 16-1.

CAUTION

Prior to installing each cable, ensure that they are orientated properly. Equipment damage may result if a cable connector is inserted upside down.

9. Insert MADTS test cable P/N 401-37845-01, P2 into bottom board edge connector J1 in back of tape drive. See Figure 16-1.
10. Set Electronics Chassis Power switch to ON position.
11. Connect tape drive power cord to power outlet.
12. Set tape drive power switch to ON position.

16.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:



13101-727
FSAS306-26

Figure 16-1. Kennedy 9000 Tape Drive Test Cable Set-Up

2.

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D TK (CR)

Printer response:

TKDIAG:

2. Input: X (CR)

Printer response:

X.

00[CTL WTA

Mount SCRATCH WRITE-PROTECTED @ LOAD

POINT, Mode OFFLINE, then Press RETURN

3. Mount Scratch Tape, Write-Protected (write-enable ring removed), on the Tandem Kennedy Tape Drive under test, and set to load point by pressing LOAD button.
4. Set tape drive to the OFFLINE mode by pressing ON LINE button (ON LINE LED is not illuminated).

5. Input: (CR)

Printer response:

STA WTB

Mode ONLINE, then press RETURN

6. Set tape drive to the ONLINE mode by pressing the on line button (ON LINE LED is illuminated).

7. Input: (CR)

Printer response:

STB WTC

Write-Enable @ EOT mode

ONLINE, then press RETURN

8. Set tape drive to OFFLINE mode, press REWIND and unload tape, insert Write-Enable ring, and reload tape.

9. Set tape drive to OFFLINE mode, press STOP button, press test MODE button, press FAST FORWARD button, wait for end of tape (EOT) light to come on.
10. Set tape drive to ON LINE mode.
11. Input: (CR)

Printer response:

```
STC RWD CBA CWA CBB CRB CBC COC
CBD CRD LEN PAT SSH RED CRP ]
```

TKDIAG:

12. Upon successful completion of this test procedure the tape drive under test is good.
13. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to Table 16-1 Tape Drive Diagnostic Error Message Description. This table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the Model 9000 Tape Drive Instruction Book TI 6490.11 for theory of operation and troubleshooting. Use accepted practices in isolation of faulty component(s).

16.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Unload scratch tape and set Tape Drive Power switch to OFF position.
5. Remove MADTS test cables from the rear of Tandem Kennedy Tape Drive and disconnect tape drive power cable.
5. If additional Kennedy Tape Drives are to be tested, return to paragraph 16.4 step 8 and proceed.
6. Remove MADTS test cables from Emulex boards in slots A3-1 and A3-2 of Electronics chassis card cage.

16.7 MADTS TANDEM KENNEDY TAPE DRIVE DIAGNOSTIC PROGRAM.

16.7.1 Calling Sequence.

DEVICE: TK
PROGRAM: DIAG

16.7.2 Function Mnemonics. The test function mnemonics used by the Kennedy tape drive diagnostic program are described below. The controller is assumed to be fully operational, since it will not respond on the bus if its automatic self test results in an error condition report.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. CTL	Emulex : TC01 Controller Functionality
b. WTA	Await -A: Drive online with write-protected scratch tape mounted
c. STA	Status-A: Drive offline with scratch tape write-protected
d. WTB	Await -B: Drive online with scratch tape write-protected, at load-point
e. STB	Status-B: Drive online with scratch tape write-protected, at load-point
f. WTC	Await -C: Drive online with scratch tape write enable, at EOT
g. STC	Status-C: Drive online with scratch tape write enabled, at EOT
h. RWD	Test Rewind
i. CBA	Test Command BACKSPACE
j. CWA	Test Command WRITE
k. CBB	Test Command BACKSPACE
l. CRB	Test Command READ
m. CBC	Test Command BACKSPACE
n. COC	Test Command OVERWRITE
o. CBD	Test Command BACKSPACE

p.	CRD	Test Command READ
q.	LEN	Test Variable Record Lengths
r.	PAT	Test Variable Data Patterns
s.	SSH	Test ShoeShine
t.	RED	Test Read-Reduction
u.	CRP	Test Record Creep

16.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which may result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic will then suspend, abort the test, loop on the function, or loop on the stimulus, depending on the options selected. Table 16-1 list all Kennedy Tape Drive Diagnostic error codes. All error codes listed with an asterisk may be reported during any function. The specific stimuli for each function and associated error data is given in Table 16-2. The address and contents of a register are normally given in the MADTS ANNOTATED DUMP (MADTS) format.

16.7.4 Error Output. Error codes and any associated data are output as follows:

Where only the Error number is reported,

ERROR #xxxx

Where supplementary CSR information is reported:

ERROR #xxxx xxxxxx xxxxxx xxxxxx xxxxxx xxxxxx xxxxxx xxxxxx

Where there is a dump of data read:

ACTUAL

XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX
XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

EXPECTED

XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX
XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX	XXXXXX

ERROR #xxxx

Error messages are given in Table 16-1.

16-1. Tape Drive Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CTL	NO-OP	<p>CTNL subrouting called to Initialize controller and validate nominal CSR content for the following registers:</p> <p>MTSXX - 'Status Reg': Bit Mask 177632 = 0</p> <p>MTCXX - 'Commond Reg' Ready bit zero</p> <p>MTBRC - 'Byte/Record Counter' = 0</p> <p>MTCMA - 'Memory Address' = 0</p> <p>MTDXX - 'Data' = 0</p> <p>MTRDX - 'Status Reg.' Bit Mask 77777 = 0</p> <p>MTRXX - 'Maintenance Reg' = 0</p>	2	Incorrect nominal controller CSR content.	<p>1st for reg. of controller are dumped:</p> <p>MTSXX MTCXX MTBRC MTCMA</p>

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTA		Requests the operator to place the system in OFF-LINE mode and mount a write protected scratch tape. No tests are conducted; the system awaits operator action and proceeds to the next function when the action has been completed.	None		
STA	SEL OFL	Select remote mode and rewind to load point.	20	'SEL' set when it should be clear.	MTSXX MTCXX MTBRC MTCMA
WTB		Requests the operator to change mode to "online" with a scratch-protected tape mounted at BOT. No tests are performed; the system resumes operation when the interaction has been completed.	None		

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
STB	RWD	CNTL subroutine is used to test for various possible error conditions.	18	'BOT' clear when it should be set.	MTSXX Reg. MTCXX
			26	'WRL' clear when it should be set.	MTBRC MTCMA
WTC		Requests the operator to change mode to "online" with a write-enabled tape mounted at EOT. No tests are performed; the system resumes operation when the interaction has been completed.	None		
STC	SPF	"Write Execute EOF Marker" to check for EOT.	14	'EOT' clear when it should be set.	MTSXV Registers MTCXV
			24	'WRL' set when it should be clear.	MTBRC MTCMA
RWD	RWD	Rewind the tape.	18	'BOT' clear when it should be set.	MTSXV Registers MTCXV MTBRC MTCMA

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CBA	SPB	Issue backspace command one time.			
CWA	WTR	Write a record containing 512 words of all "1's" to the tape.			
CBB	SPB	The drive should backspace to the BOT and the BOT indicator should light.			
CRB	RDR	Read the record from the tape and compare to what was written. If they are not the same, issue an error code.	36	'DATA COMPARE' error (s/w detected).	Expected data Actual data MTSXX MTCXX MTBRC MTCMA

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CBC	SPB	The drive should backspace to BOT and the BOT indicator should light.			
COC	WTO	Overwrite the record. Determine whether any errors were encountered during the operation.			
CBD	SPB	The drive should backspace to the BOT and the BOT indicator should light.			
CRD	RDR	Read the record from the tape and compare with what was written to tape. If they are not the same, issue an error code.	36	'DATA COMPARE' error (software detected).	Expected data Actual data MTSXX Registers MTCXX MTBRC MTCMA

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LEN	RWD	Rewind the tape to BOT. If no BOT is observed an error code will be issued.	18	'BOT' clear when it should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
	WTR	Write 25U records consisting of all '1's' with record size starting at 1 word to 256 words.			
	RWD	Rewind to BOT. If BOT is not found, an error code is issued.	18	'BOT' clear when it should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
	RDR	Read the 256 records off tape and check to see if the data is all '1's'.	36	'DATA COMPARE' error.	Expected data Actual data MTSXX Reg MTCXX MTBRC MTCMA

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
	SPB	Backspace 256 records.			
PAT	RWD	Rewind to BOT. Failure to read BOT will cause an error code to be issued.	18	'BOT' clear when it should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
	WTR	A group of 256 records containing 256 bytes all the same value within the same record will be written to tape. Each record will consist of a different byte value ranging from 1-256.			
	RWD	Rewind to BOT. Failure to read BOT will cause an error code to be issued.	18	'BOT' clear when it should be set.	MTSXX Reg MTCXX MTBRC MTCMA

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
	RDR	Read the previously written records, comparing them to what should be on tape. Failure to verify will cause data comparison error.	36	'DATA COMPARE' error (software detected).	Expected data Actual data MTSXX Reg MTCXX MTBRC MTCMA
SSH	RWD Shoe-shine	Rewind to BOT. Repeats this sequence 256 times. Write a 1 byte record. Backspace 1 record. Read 1 record. Check data.	18	'BOT' clear when should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
		Vary data pattern (1-256).	36	'DATA COMPARE' error (software detected).	

Table 16-1. Tape Drive Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
RED	RWD WTR	The tape is rewound to BOT. A record containing a pattern of all "1's" is then written to the tape. The record is read and backspaced for 10 repetitions, at each pass comparing the data recovered with that recorded.	18	'BOT' clear when should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
			36	'DATA COMPARE' error (software detected).	Expected data Actual data MTSXX Reg. MTCXX MTBRC MTCMA
CRP	Record Creep	Rewind to 'BOT'. Write 2 records 256 bytes each, first all '1's' and second all zeroes. For U4 repetitions: Backspace to beg of second record delay 10 sec. Overwrite 2cc record with some data. End for. Rewind to 'BOT'. Read 1st record and compare data. Read 2nd record and compare data.	18	'BOT' clear when should be set.	MTSXX Reg. MTCXX MTBRC MTCMA
			36	'DATA COMPARE' error (software detected).	Expected data Actual data MTSXX Reg. MTCXX MTBRC MTCMA

Table 16-2. Kennedy Diagnostic Error Codes

*	0	CONTROLLER-ACCESS BUS TIMEOUT ERROR
*	2	INCORRECT NOMINAL CONTROLLER CSR CONTENT
*	4	INCORRECT NOMINAL CONTROLLER INTERRUPT GENERATION
*	6	'OPERATION INCOMPLETE' ERROR
*	8	'EOF' SET WHEN SHOULD BE CLR
	10	'EOF' CLR WHEN SHOULD BE SET
*	12	'EOT' SET WHEN SHOULD BE CLR
	14	'EOT' CLR WHEN SHOULD BE SET
*	16	'BOT' SET WHEN SHOULD BE CLR
	18	'BOT' CLR WHEN SHOULD BE SET
	20	'SEL' SET WHEN SHOULD BE CLR
*	22	'SEL' CLR WHEN SHOULD BE SET
*	24	'WRL' SET WHEN SHOULD BE CLR
	26	'WRL' CLR WHEN SHOULD BE SET
*	28	'DATA-CHECK' ERROR (H/W DETECTED)
*	30	'PARITY ERROR' (H/W DETECTED)
*	32	'RECORD LENGTH ERROR'
*	34	'BAD TAPE ERROR'
	36	'DATA COMPARE' ERROR (S/W DETECTED)
*	38	'SYSTEM' ERROR (NON-SPECIFIC PROBLEM--SEE CSR CONTENT)

* Error may be reported during any function

SECTION XVII
LRU TEST PROCEDURES
AMPEX 9300 DISK DRIVE

17.1 GENERAL. This section contains test procedures for the Tandem Ampex Disk Drive Model 9300, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

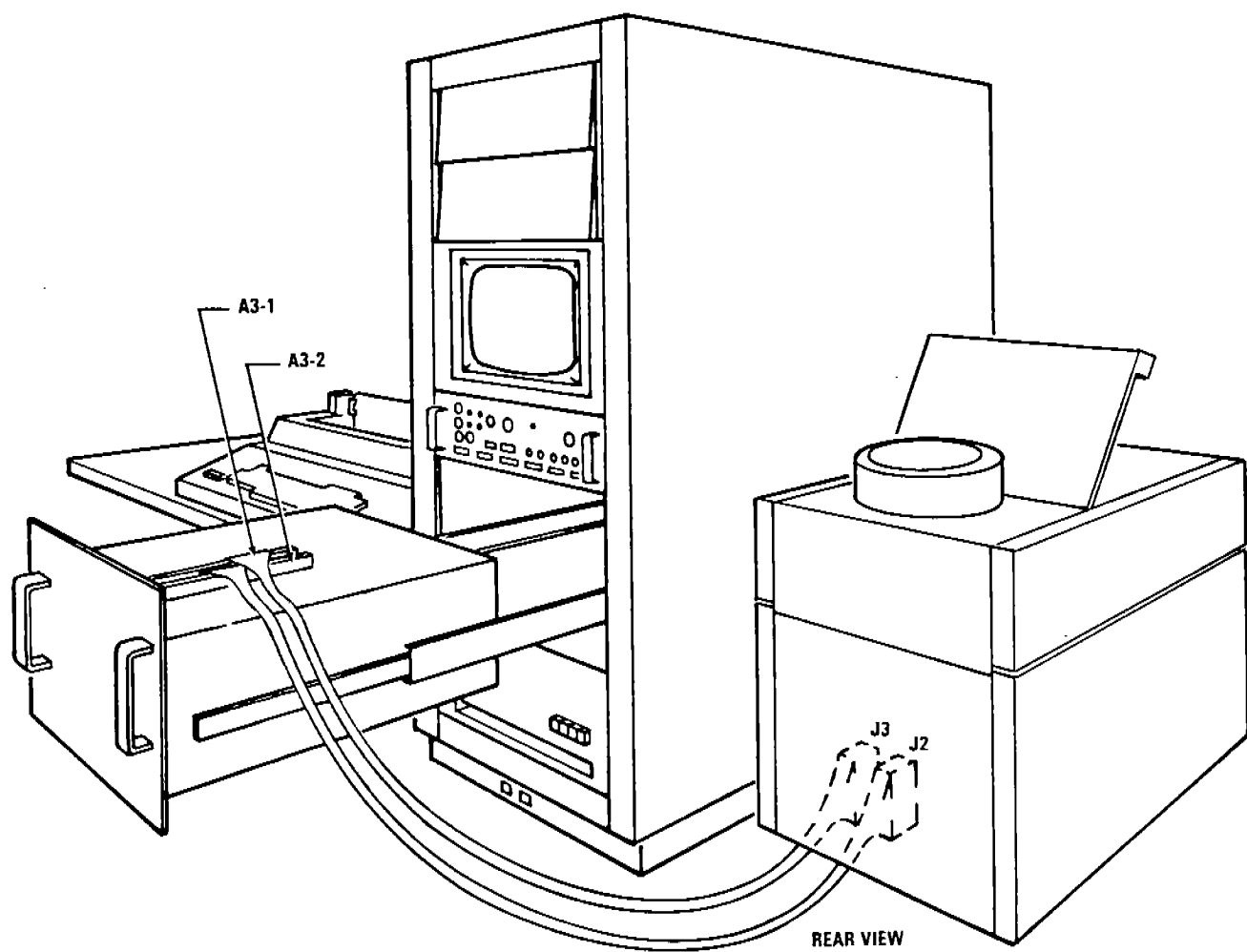
17.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Tandem Ampex 9300 Disk Drive:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
MADTS Test Cable	E-Systems P/N 401-37848-01
MADTS Test Cable	E-Systems P/N 401-37847-01
MADTS Formatted Scratch Disk	
Emulex SC01/E2 Controller	SC01/E2
Ampex Terminator	3305667-01

Tools other than standard shop tools are not required for test of the disk drive.

The Ampex Disk Drive requires 3 phase, 208 VAC, 20 amp power for operation and test.

17.3 OTHER DOCUMENTATION. Refer to DM 9300 TD Disk Drive Instruction Book (TI 6490.12) for detailed information on the Tandem Ampex 9300 Disk Drive.



FSAS306-10

Figure 17-1. Ampex 9300 Disk Drive Test Set-Up

17.4 PREPARATION FOR TEST. To prepare the disk drive for test, follow the instructions listed below and see Figure 17-1.

1. Verify that System Power switch is set to ON position.
2. Set Electronics Chassis Power switch to OFF position.
3. Verify that Emulex Controller SC01-B1, is in slot A3-1 and A3-2 of Electronics Chassis card cage.
4. Insert MADTS test cable P/N 401-37848-01, P1 into J1 of Emulex board in A3-1.
5. Insert MADTS test cable P/N 401-37847-01, P1 into J1 of Emulex board in A3-2.
6. Insert MADTS test cable P/N 401-37848-01, P2 into J2 of Tandem Ampex Disk Drive.
7. Insert MADTS test cable P/N 401-37847-01, P2 into J3 of Tandem Ampex Disk Drive.
8. If there is no terminator, P/N 3305667-01 in J1 of Ampex Disk Drive, install one.
9. Connect Ampex Disk Drive power cord to power outlet.
10. Set the Electronics Chassis Power switch to ON position.
11. Set Tandem Ampex Disk Drive power switch to ON position.

17.5 TEST PROCEDURES. When the Power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

KT *
KP *
MP *.....
MR*...
MS *.....
RL *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

: D RL.

RL : B.

RT-115J (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

KT *
AN
CI
DL
FP
IP *..
KB *
KP *
LA *
LP *
MP *.....
MR*...
MS *.....
MX *.....
RL *???.
TA *
TK *

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D TA (CR)

Printer response:

TADIAG:

2. Input: X (CR)

Printer response:

X.

00 [WTA

Mount Standards/Scratch Pack, Read-Only,
ID 0, Mode OFFLINE, then press RETURN

3. Place the Ampex Disk Drive in the OFFLINE mode by placing START/STOP rocker switch to STOP position.
4. Open Ampex Disk Drive front panel (pull manual release handle to open disk housing).
5. Mount a scratch disk.
6. Input: (CR)

Printer response:

STA WTB

Mode ONLINE, then press RETURN

7. Set the Ampex Disk Drive to the ONLINE mode by placing the START/STOP rocker switch to START position after READY light is illuminated.

NOTE

The following test will run for
approximately 5 minutes.

8. Input: (CR)

Printer response:

STB FLY SCR TRK CYL FLW WTD
Mode Read/Write, Online, then
Press RETURN

9. Set the Ampex Disk Drive to the Read/Write mode by placing the READ ONLY R/W rocker switch to R/W position.

NOTE

The following test will run for approximately 10 minutes

10. Input: (CR)

Printer response:

STD WRT IFT FMT

TADIAG:

11. Place the Ampex Disk Drive in the OFFLINE mode by placing the START/STOP rocker switch to STOP position.
12. Move the cable from J3 to J6 in the Ampex Disk Drive.
13. Move the cable from J2 to J5 in the Ampex Disk Drive.
14. Move the terminator from J1 to J4 in the Ampex Disk Drive.
15. Input: S -IFR-FMT (CR)

Printer response:

TADIAG:

16. Repeat steps 3 through 10
17. Upon successful completion of this test procedure the Ampex Disk Drive under test is good.
18. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 17.7 and Table 10.2, Ampex Disk Drive Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the DM9300TD Disk Drive Instruction Book (TI 6490.12) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

17.6 POWER DOWN SEQUENCE.

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.

3. Remove MADTS test cables from rear of Ampex Disk Drive.
4. If terminator was installed, remove it.
5. If another Ampex Disk Drive is to be tested, return to paragraph 17.4 and proceed.
6. Remove MADTS test cables from Emulex boards in slots A3-1 and A3-2 of Electronics Chassis MADTS card cage.
7. Remove Emulex boards from slots A3-1 and A3-2 of Electronics Chassis.

17.7 MADTS TANDEM AMPEX DISK DIAGNOSTIC PROGRAM.

17.7.1 Calling Sequence.

Device: TA
Program: DIAG

17.7.2 Function Mnemonics. The test function mnemonics used by the Ampex Disk Drive diagnostic program are described in the following list in the order of their occurrence. These tests require operator intervention and mounting a scratch disk formatted by the Emulex Controller. The controller is assumed to be fully operational, since it will not respond on the bus if its automatic self-test results in an error condition report.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. WTA	Await DRIVE OFFLINE with scratch pack.
b. STA	Test nominal OFFLINE DRIVE status.
c. WTB	Await DRIVE ONLINE with scratch pack.
d. STB	Test nominal ONLINE DRIVE status.
e. FLY	Test head-flying capability.
f. SCR	Test ability to search for and read sectors.
g. TRK	Test ability to select tracks and read sectors.

PROGRAM FUNCTIONS (Continued)

<u>Mnemonic</u>	<u>Function</u>
h. CYL	Test ability to seek cylinders and read sectors.
i. FLW	Test ability to follow cylinder.
j. WTD	Await DRIVE ONLINE with scratch park.
k. STD	Test nominal ONLINE drive status.
l. WRT	Test ability to write sectors (various).
m. IFR	Test adjacent-cylinder READ/WRITE interference.
n. FMT	Test and format pack.

17.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which may result in an error condition. Detection of an error after excitation has been applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. Table 17-1 list all Ampex Disk Drive diagnostic error codes. All error codes listed with an asterisk may be reported during any function. The specific stimulus for each function and its associated error data is given in Table 17-2. The address and contents of a register are normally given in the MADTS ANNOTATED DUMP format.

17.7.4 Error Output. When errors are declared, the error number and scratch pad data are output in the following format:

```
ERROR      #xxxx      aaaa  bbbb  cccc  dddd  eeee  ffff  gggg
```

```
where:      xxxx is the error number
```

```
Scratch:    aaaa is the current cylinder number
Pad          bbbb is the current track number
             cccc is the current sector number
             dddd is the previous cylinder number
             eeee is the previous track number
             ffff is the previous sector number
             gggg is the phase number (if any)
```

Additional annotated data is output when header errors are declared:

Header	Word 1	Word 2
	zzzz	yyyy

where: zzzz and yyyy are header values

Additional annotated data is output when data comparison errors are detected during the WRT function:

Actual	mmmm
Expected	nnnn

where: mmmm is the value read from this current sector
nnnn is the expected value (data pattern)

Control/Status Register data is displayed using the following format:

AMPEX CSR BANK DUMP

RMCS1	RMWC	RMBA	RMDA	RMCS2	RMDS	RMER1	RMAS
****	****	****	****	*****	****	*****	****
RMLA	RMOF	RMDC	RMER2	RMEC1	RMEC2		
****	****	****	*****	*****	*****		

where **** is the current contents of a register.

CSR content is reported by the Bit Field Dump. The following field content provides the information needed to interpret the conditions pertaining at the time of the dump.

<u>MNEMONIC</u>	<u>ADDRESS</u>	<u>OCTAL/BIT</u>	<u>BIT Definition</u>
RMCS1	176700	100000/15 040000/14 020000/13 010000/12 004000/11 001000/9 000400/8 000200/7 000100/6	Special Condition Transfer Error Massbus Control Bus Parity Error Port Select Drive Available Extended Bus Address Extended Bus Address Ready Interrupt Enable
		BIT 5 thru BIT 0 are functional combinations in Octal	Functions
		01 03 05 07 11 13 15 17 21 23 31 51 53 61 63 71 73 75 77	No operation Unload (Standby) (Opt) Seek Command Recalibrate Drive Clear Release (Dual Port Operation) Offset Command Return to Centerline Read-IM Preset Pack Acknowledge Search Command Write Check Data Write Check Header and Data Write Data Write Header and Data Read Data Read Header and Data Boot (Optional) Format (Optional)
RMWC	176702	BIT 15 thru BIT 0	Emulex Word Count
RMBA	176704	BIT 15 thru BIT 0	Emulex Memory Address
RMDA	176706	010000/12-000400/8 000020/4-000001/0	Track Address Sector Address

<u>MNEMONIC</u>	<u>ADDRESS</u>	<u>OCTAL/BIT</u>	<u>BIT Definition</u>
RMCS2	176710	100000/15	Data Late
		040000/14	Write Check Error
		020000/13	Unibus Parity Error
		010000/12	Nonexistent Drive
		004000/11	Nonexistent Memory
		002000/10	Program Error
		001000/9	Missed Transfer
		000400/8	Massbus Data Bus Parity
		000200/7	Output Ready
		000100/6	Input Ready
		000040/5	Controller Clear
		000020/4	Parity Test
		000010/3	Unibus Address Increment
RMDS	176712		Inhibit
		000004/2-000001/0	Unit Select
		100000/15	Attention Active
		040000/14	Error
		020000/13	Positioning in Progress
		010000/12	Medium On-Line
		004000/11	Write Lock
		002000/10	Last Sector Transfer
		001000/9	Programmable
		000400/8	Drive Present
		000200/7	Drive Ready
RMER1	176714	000100/6	Volume Valid
		000001/0	Offset Mode
		100000/15	Data Check
		040000/14	Unsafe
		020000/13	Operation Incomplete
		010000/12	Drive Timing Error
		004000/11	Write Lock Error
		002000/10	Invalid Address
		001000/9	Address Overflow Error
		000400/8	Header CRC Error
		000200/7	Header Compare Error
		000100/6	ECC Hard Error
		000040/5	Write Clock Fail
Refused		000020/4	Format Error
		000010/3	Parity Error
		000004/2	Register Modification
		000002/1	Illegal Register
		000001/0	Illegal Function
RMAS	176716	002000/10-	Sector Counter
		000100/6	

<u>MNEMONIC</u>	<u>ADDRESS</u>	<u>OCTAL/BIT</u>	<u>BIT Definition</u>
RMDB	1767222	100000/15- 000001/0	Data Buffer
RMMR1	176724	001000/9 000400/8 000200/7 000100/6 000010/3 000001/0	Maintenance Unit Ready Maintenance On Cylinder Maintenance Seek Error Maintenance Drive Fault Maintenance Write Protect Diagnostic Mode
RMDT	176726		Drive Type Register
RMSN	176730		Serial Number Register
RMDF	176732	010000/12 004000/11	Format Bit Error Correction Code
Inhibit		002000/10 000200/7	Header Compare Inhibit Offset Direction
RMDC	176734	001000/9-000001/0	Desired Cylinder Address
RMHR	176736		Holding Register
RMMR2	176740		Maintenance Register
RMER2	176742	100000/15 040000/14 020000/13 010000/12 004000/11 002000/10 001000/9 000400/8 000200/7 000010/3	Bod Sector Error Seek Incomplete Operator Plug Error Invalid Command Loss of Sector Clock Loss of Bit Clock Multiple Drive Select D.C. Power Unsafe Device Check Data Parity Error
RMEC1	176744	010000/12- 000001/0	ECC Position
RMEC2	176746	002000/10- 000001/0	Error Pattern

Table 17-1. Ampex Diagnostic Error Codes

*	0	CONTROLLER-ACCESS BUS TIMEOUT ERROR
*	2	CONTROLLER NOT READY IN ALLOTTED TIME
*	4	INCORRECT NOMINAL CONTROLLER CSR CONTENT
*	6	INCORRECT NOMINAL CONTROLLER INTERRUPT GENERATION
*	8	WRITE-CHECK ERROR
*	10	UNIT ADDRESSING ERROR (NED OR MDS)
	12	ATTN SET WHEN EXPECTING A CLEAR
	14	ATTN CLEAR WHEN EXPECTING SET
	16	UNIT RDY SET WHEN EXPECTING CLR
	18	UNIT RDY CLR WHEN EXPECTING SET
	20	WRITE PROT SET WHEN EXPECTING CLR
	22	WRITE PROT CLR WHEN EXPECTING SET
	24	UNIT CYCLED WHEN SHOULD NOT
	26	UNIT NOT CYCLED WHEN SHOULD HAVE
*	28	DATA CHECK ERROR (H/W ECC DETECTED)
*	30	OPERATION INCOMPLETE ERROR (SECTOR SEARCH TIMEOUT)
*	32	DRIVE TIMING ERROR (MISSING HDR OR DATA SYNC PATTERNS)
*	34	HDR CRC ERROR (H/W DETECTED)
*	36	HDR COMPARE ERROR (H/W DETECTED SEARCH ERROR)
*	38	BAD SECTOR ERROR (H/W DETECTED SECTOR MARKER BAD)
*	40	SEEK INCOMPLETE ERROR (H/W DETECTED SEEK TIMEOUT)
*	42	LOSS OF SECTOR CLOCK ERROR (H/W DETECTED)
*	44	LOSS OF BIT CLOCK ERROR (H/W DETECTED)
*	46	DEVICE CHECK (H/W DETECTED DRIVE FAULT)
*	48	DATA COMPARE ERROR (S/W DETECTED)
*	50	SYSTEM ERROR (NONSPECIFIC PROBLEM -- SEE CSR CONTENT)

Table 17-2. Tandem Ampex Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTA		Requests the operator to place the system in off-line mode and to mount a scratch disk. No tests are conducted; the system awaits operator action and proceeds to the next function when the action has been completed.		None	None
STA	No-Op	Perform a no-op function and verify that the controller reports nominal conditions in its CSRs.		None	
	Check Status Off-line	Stimulus checks driver status. If unit ready is detected (unit is on-line), then the stimulus reports a Unit Ready (MOL) error.	16	Unit RDY SET - when expecting CLR-unit was supposed to be on-line but was reported off-line.	Unit Ready set when clear expected.

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTB		Requests the operator to change mode to on-line and then resumes operation when the interaction has been completed.		None	None
STB	Check Status On-Line	Stimulus verifies that the controller senses an on-line condition for the drive and that write protect (Read-Only) is in effect for the drive.	18	Unit RDY CLR - when expecting SET, unit was supposed to be on-line, but was reported off-line.	Unit Ready clear when expecting set (drive is not available).
			22	Write PROT CLR - when expecting SET. Write protect logic allowed write to disk after operator was instructed to set write protect to ON.	Write Protect clear when expecting set (Read-only not in effect).

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
FLY	Increment Seek	Performs an increment seek between cylinders 0 and each value up to 814, then between cylinder 814 and each value until cylinder 0. (Example; 0, 1, 2..... 0, 813, 0, 814, 812).		None	
	Cross-Seek	This stimulus starts with the cylinder bounds of the seek being 0 and 814 and squeezes them to 407, and expands the bounds back out to 0 and 814. (Example; 0, 814, 1, 813, 406, 408, 407, 407, 408).		None	
	Stagger-Seek	This stimulus starts out at cylinder 0. It then seeks forward 2 and back 1 until it reaches the last cylinder. It moves to cylinder 0 in the same way. (Example; 0, 2, 1, 3 813, 812, 814, 4, 2, 3, 1, 2, 0).		None	

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SCR	Cali-brate	Positions the heads over cylinder 0.		None	
	Search	For cylinder 0 track 0 only read data and header for all sectors display header word values if an error is detected.			Display word 1 of header. Display word 2 of header.
TRK	Cali-brate	Home header over cylinder 0.		None	
	Read Data and Header	Each track is selected and its first sector is read from cylinder 0. Header data will be reported along with any detected errors.			Display word 1 of header. Display word 2 of header.
CYL	Increment Seek/Read	Performs an increment- seek between cylinders 0 and each value up to 814, then between 814 and each value until cylinder 0. Seek the cylinder, then read data and header values and report errors. (Example; 0, 1, 0, 2..... ...0, 813, 0, 814).		None	If header error: Display word 1 of header. Display word 2 of header.

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CYL	Cross-Seek then Read	Starts with the cylinder bounds of the seek being 0 and 814 and sequences them to 407 and expands the bounds back to 0 and 814. Seek the cylinder, then read data and header values and report errors. (Example: 0, 814, 1, 813,406, 408, 407, 407, 408).		None	If header error: Display word 1 header. Display word 2 header.
	Stagger Seek/Read	This stimulus starts out at cylinder 0, then seeks forward 2 and back 1 until it reaches the last cylinder. It moves to cylinder 0 in the same way. (Example: 0, 2, 1, 3813, 814, 812.....4, 2, 3, 1, 2, 0).		None	If header error: Display word 1 header. Display word 2 header.

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
FLW	Cursory-Seek	This stimulus seeks for one of three cylinder positions (0, 407, 813).		None	
	Calibrate then Read	For each of the cylinder values selected in the Cursory-seek stimulus, this stimulus performs a loop to read data and header values. First the heads are homed to cylinder 0 (calibrate operation). Next the stimulus attempts to read the first sector of every track and to check for errors 64 times. The read operation should implicitly seek for the targeted cylinder. The loop is terminated if an error is detected.		None	If header error: Display word 1 of header. Display word 2 of header.

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTD		The operator is requested to enable WRITE (Read/Write mode). Upon receipt of RETURN the test operation continues.		None	None
STD	Medium is On-Line	The controller is checked to ensure that the medium is on-line, otherwise an MOL error is reported.	18	Unit RDY CLR when expecting SET, unit was supposed to be on-line but was reported off-line.	Unit Ready Clear when expecting set.
	Write Lock	Verifies that WRITE is enabled otherwise it reports a write lock error.	20	WRITE PROT SET when expecting CLR, write protect logic did not allow write after operation was instructed to set write protect to off.	Write Protect set when expecting clear.

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WRT	Write Data Pattern	Performs a loop to test the write/readback functions. It first employs the cursory seek algorithm to select one of three cylinder positions (0, 407, 813). For each selected position, it moves the head back to cylinder 0 (calibrate) and writes a data pattern to the first sector. The write operation should implicitly seek for the selected cylinder position. The stimulus then attempts to read the sector and then compares the read data to expected data. The stimulus reports comparison errors. The loop is continued until each track and each cursory cylinder position is tested or an error is detected.	48	DATA COMPARE error (S/W detected). Data read back after a WRITE found erroneous.	Data compare error. Actual Sector Data Expected Sector Data Cylinder Number Track Number Sector Number

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IFR	Inter-fer-ence	<p>Stimulus is performed in six phases that test the immunity to data interference between adjacent cylinders. IFR uses the cursory-seeking algorithm to select each of the three representative cylinder positions (0, 407, 813). For each of these cylinders the stimulus performs the following loop:</p> <ol style="list-style-type: none"> 1. During phase 1, the stimulus creates a data pattern and writes the pattern to the current sector and track. Then a write check is performed. (Reads data just written and compares it to pattern in memory). All sectors and tracks are tested. 			<p>Write check error. Phase Number 1 - 6. Error code assigned by CNTL subroutine. (RMCS2-14)</p>

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IFR		<p>2. During phase 2, the stimulus increments the cylinder no, then writes a complemented data pattern to the current sector and track. A write check is also performed to ensure data integrity. All sectors and tracks are tested (until) an error is detected.</p> <p>3. Phase 3 increments the cylinder no. and tests the original cylinder against the original data pattern using only the write check operation (on all tracks and sectors).</p> <p>4. Phase 4 tests the adjacent cylinder by incrementing the cylinder no. and using the original data pattern by employing both write and write check operations.</p>		:	

Table 17-2. Tandem Ampex Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IFR		<p>5. During Phase 5 the stimulus increments the cylinder no. and writes the complemented data pattern. Both write and write check operations are used on each sector and track.</p> <p>6. Phase 6 increments the cylinder no. and checks the original data pattern using only the write check operations.</p>			
FMT	Format	Stimulus attempts to format the disk pack by issuing a controller format command.		None	

SECTION XVIII
LRU TEST PROCEDURES
LA34-AA/LA100-CA INPUT/OUTPUT TERMINAL

18.1 GENERAL. This section contains the LRU test procedures for LA34-AA/LA100-CA Input/Output Terminal printer/KBD as tested by the MADTS. The test is conducted under diagnostic software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

18.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for testing the LA34/LA100:

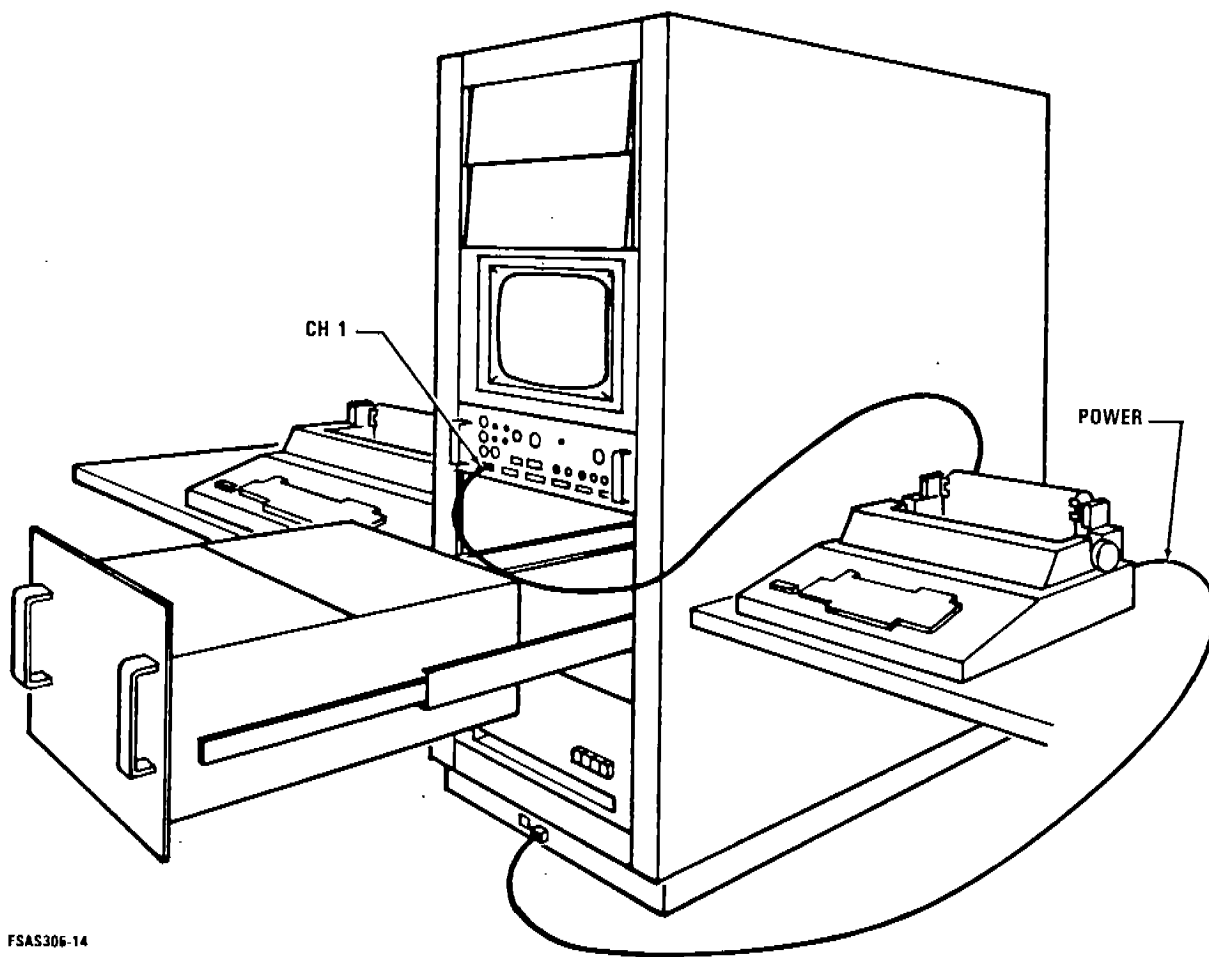
<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
MADTS Test Cable	E-Systems P/N 401-37126-07

Tools other than standard shop tools are not required in test of the LA34/LA100.

18.3 OTHER DOCUMENTATION. Other documentation required for test of the LA34/LA100 is the LA34 Instruction Book TI 6490.6 and LA100 Instruction Book TI 6490.39.

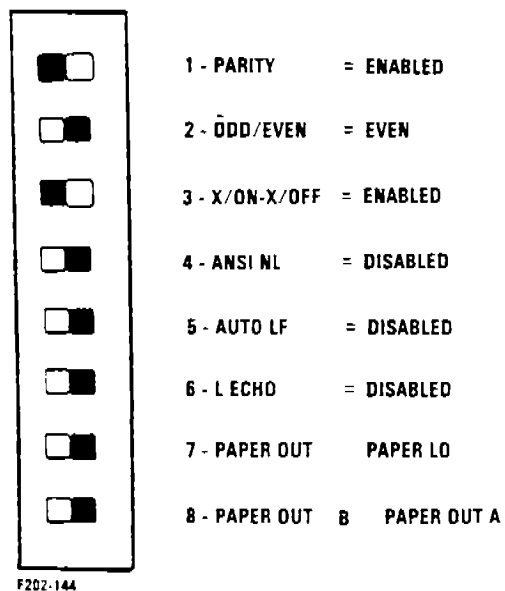
18.4 PREPARATION FOR TEST. To prepare the LA34/LA100 for test, follow the instructions listed below and see Figure 18-1.

1. Inspect LA34/LA100 visually for defects.
2. Verify that switch settings are as in Figure 18-2.
3. Install printer paper in LA34/LA100 (unit under test).
4. Verify that System power switch is in ON position.
5. Set Electronics Chassis power switch to OFF.
6. Connect MADTS test cable 401-37126-07, P1, to Channel 1 on I/O Control Panel.
7. Connect MADTS test cable 401-37126-07, P2, to RS-232 port on LA34/LA100 (unit under test).
8. Set LA34/LA100 (unit under test) switches as follows:
 - a. POWER switch to ON.
 - b. SPEED switch to 300 baud
 - c. LINE/LOC switch to LINE



FSAS306-14

Figure 18-1. LA34/LA100 Terminal Test Set-Up



NOTE: SWITCH IS ACCESSED THROUGH OPENING UNDER PRINT HEAD.

Figure 18-2. LA34/LA100 Switch Settings

18.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

2.
Q

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D LA (CR)

Printer response:

LADIAG:

2. Input: X (CR)

Printer response:

X.
00 [DAT PRI PIT KEY

NOTE

The following instructions are also printed on the LA34/LA100 (unit under test).

3. Verify that the LA34/LA100 (unit under test) printout matches the sample printout in Figure 18-3.
4. With CAPS LOCK on, press the following key sequences on the LA34/LA100 (unit under test):
 - ESC to BACKSPACE
 - TAB to DELETE (Skip RETURN key)
 - A to I (including RETURN key)
 - Z to LINE FEED and SPACE bar
5. The LA34/LA100 (unit under test) will echo all printable characters entered:


```
1234567890-=' QWERTYUIOP[ ]ASDFGHJKL;'
ZXCVBNM,./
```
6. While depressing the control (CNTL) key on the LA34/LA100 (unit under test) depress the A key.
7. While pressing the left SHIFT key on the LA34/LA100 (unit under test), depress the I key (an exclamation point will be printed).
8. While pressing the right SHIFT key on the LA34/LA100 (unit under test), press the 5 key (a percent sign will be printed).
9. Printer response:

] -

PRINTER TEST
X X X X X X X

VERTICAL AND HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A HORIZONTAL PITCH TEST
THIS IS A HORIZONTAL PITCH TEST

THIS IS A VERTICAL PITCH TEST
THIS IS A VERTICAL PITCH TEST
THIS IS A VERTICAL PITCH TEST

THIS IS A VERTICAL PITCH TEST
THIS IS A VERTICAL PITCH TEST

THIS IS A VERTICAL PITCH TEST
THIS IS A VERTICAL PITCH TEST

Figure 18-3. LA34/LA100 Test Print Pattern

11. The LA34/LA100 diagnostic test is complete. If no errors were reported by MADTS, the LA34/LA100 is good.
12. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 18.7 and Table 18-1, LA34/LA100 Error Messages. This table lists the test function, stimulus, and other information that may be contained in messages generated by the diagnostic program. Refer to the LA34 Instruction Book (TI 6490.6) or LA100 Instruction Book (TI 6490.39) for assistance in troubleshooting. Use accepted practices in isolation of faulty component(s).

18.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set LA34/LA100 Power switch (unit under test) to OFF.
2. Remove MADTS test cable 401-37126-07, P2 from RS-232 port on LA34/LA100 under test.
3. If an additional LA34/LA100 is to be tested, return to paragraph 18.4 and proceed.
4. Set momentary BOOT/HALT switch to HALT Position.
5. Set Electronics Chassis POWER switch to OFF position.
6. Remove MADTS test cable 401-37126-07 from Channel 1 on I/O Control Panel.

18.7 MADTS LA34/LA100 DIAGNOSTIC PROGRAM.

18.7.1 Calling Sequences.

Device: LA
Program: DIAG

18.7.2 Function Mnemonics.

The test function mnemonics used by the LA34/LA100 diagnostic program are as follows. Unless otherwise noted, functions are enabled by default for the manual test mode and disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. DAT	Ensures that the LA34/LA100 can receive and transmit serial data.
b. ERR	Ensures that the XON and XOFF characters are properly sent by the LA34/LA100 printer. Disabled by default.
c. PRI	Tests the forward and backward movement of the LA34/LA100 print head.
d. PIT	Tests the horizontal and vertical pitch ranges of the printer.
e. KEY	Ensures that each key on the LA34/LA100 keyboard generates the proper ASCII value. This function is disabled by default.
f. ECH	Allows the operator to exercise the keys of the LA34/LA100 keyboard. This function is disabled by default.

18.7.3 Function Stimuli Descriptions.

A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data are given in Table 18-1. The address and contents of a CSR is normally given in the Bit Field Decomposition format.

18.7.4 Error Output

Error codes and any associated data are output in the following form:

```
ERROR #xxxx      aaaaaa  bbbbbb
```

where:

```
xxxx      is the error number
aaaaaa    is the first output parameter
```

The number of output parameters will vary from 0 to 2 depending on the error. Additional error data may be given in an annotated dump format as follows:

Key #	EXPCTD	ACTUAL
000000	000100	000101
000001	000101	000102
000002	000102	000103
000003	000103	000104
000004	000104	000105

The error codes used by the MADTS LA34/LA100 diagnostic program and their associated output parameters are given in Table 18-1.

Table 18-1. LA34/LA100 Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DAT	Data Transfer Test	A reset command is sent to the LA-34/LA100 which causes an XON to be returned. A terminal ID request is then sent to the LA-34/LA100. A terminal ID 10 sequence is expected back from the LA-34/LA100. The sequence consists of an escape character followed by 73;l. Any trailing characters are ignored.	0	Device did not respond when queried.	CSR contents (BFD)
			2	Terminal ID sent by the device is not correct.	Terminal ID received
			4	A parity error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the device.	CSR contents (BFD)
ERR	Error Test	A reset command is sent to the LA-34/LA100 which causes an XON to be returned. A series of command sequences are sent to the LA-34/LA100 which will cause it	10	An expected XON character was not received within the allotted amount of time.	None

Table 18-1. LA34/LA100 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		to exceed its buffer overflow threshold, resulting in an XOFF character being output over the serial line. Upon receipt of the XOFF character, character transmission is suspended until an XON is generated, indicating that the LA-34/LA100 has adequate buffer space for serial input.	12	An expected XOFF character was not received within the allotted amount of time.	None
PRI	Print Head Test	A reset command is sent to the LA-34/LA100 which causes an XON to be returned. A 'Printer Test' message is printed on the LA-34/LA100, indicating test initiation.	4	A parity error occurred during receipt of a serial character from the device.	CSR contents (BFD)
		Underline characters are printed at the column positions that will be used to terminate print head movement for this test. The print head is moved various amounts from the right or left margin before printing either a "/" or "1", depending on the origin. Movement from the left margin is accomplished by printing blanks and is terminated with a "/", while movement from	6	An overrun error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			10	An expected XON character was not received within the	None

Table 18-1. LA34/LA100 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		the right margin is accomplished with backspace characters and ends with a "l". The resulting line of output is similar to that shown below and must be verified by the specialist. <u>X</u> <u>X</u> <u>X</u> <u>X</u> <u>X</u> <u>X</u> <u>X</u>		allotted amount of time.	
PIT	Pitch Test	A reset command is sent to the LA-34/LA100 which causes an XON to be returned. A "Vertical and horizontal pitch test" message is printed on the LA-34/LA100, indicating test initiation.	4	A parity error occurred during receipt of a serial character from the device.	CSR contents (BFD)
		A progression of horizontal pitch occurs by printing "this is a horizontal pitch test" with a single pitch change every other time it is repeated. Each line printed at a new pitch is followed by two line feeds and is repeated at the same pitch. This pattern repeats for the full range of horizontal pitch. Vertical pitch is constant during the horizontal pitch test. The	6	An overrun error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			10	An expected XON character was not received within the allotted amount of time.	None

Table 18-1. LA34/LA100 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		sequence is repeated for the vertical pitch test, with the vertical pitch being incremented, and the horizontal pitch being constant. "This is a vertical pitch test" is used as the output line.			
KEY	Caps-locks Key Test	A message is output to the LA-34/LA100 giving the operator test instructions which include pressing the caps - lock key and typing keys on the keyboard, going from left to right and top to bottom. The keys must be typed in the indicated sequence. Characters typed are echoed to the LA-34/LA100. After the sequence has been completed, any errors are reported. If a key is not typed within 5 minutes, the function is terminated with any accumulated errors reported.	18	One or more character codes do not match those in the predetermined key sequence.	Key number Expected character Actual character (Read from the serial interface data buffer).
	Control Key Test	A message is output to the LA-34/LA100 instructing the operator to type the control and 'A' keys si-	4	A parity error occurred during the receipt of a serial character from the device.	CSR contents (BFD)

Table 18-1. LA34/LA100 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		multaneously. The resulting key code is verified. If a key is not typed within 5 minutes, the function is terminated.	6	An overrun error occurred during the receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during the receipt of a serial character from the device.	CSR contents (BFD)
			14	A character code other than a control-A (SOH) was received.	Expected character Actual character
Shift Key Test		A message is output to the LA-34/LA100 instructing the operator to type the shift and 1 keys simultaneously. The resulting keycode is echoed to the LA-34/LA100 and verified. A message is then output to the LA-34/LA100 which instructs the operator to type the shift and 5 keys simultaneously. The resulting keycode is also echoed and verified. If a key is not typed within 5	4	A parity error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			6	An overrun error occurred during receipt of a serial character from the device.	CSR contents (BFD)
			8	A framing error occurred during re-	CSR contents (BFD)

Table 18-1. LA34/LA100 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		minutes, the function is terminated.	16	ceipt of a serial character from the device. An invalid shifted character was received.	Expected character Actual character
ECH	Echo Character	Each key typed at the LA-34/LA100 keyboard by the specialist is echoed to the LA-34/LA100 printer. Non-displayable keycodes will have their octal value printed. Typing the delete key before any key will also cause that key's octal value to be printed. If a key is not typed within 5 minutes, the function is terminated.	4 6 8	A parity error occurred during receipt of a serial character from the device. An overrun error occurred during receipt of a serial character from the device. A framing error occurred during the receipt of a serial character from the device.	CSR contents (BFD) CSR contents (BFD) CSR contents (BFD)

SECTION XIX
LRU TEST PROCEDURES
DMA-QB

19.1 GENERAL. This section contains the test procedures for the DMA-QB assembly, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

19.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the DMA-QB assembly:

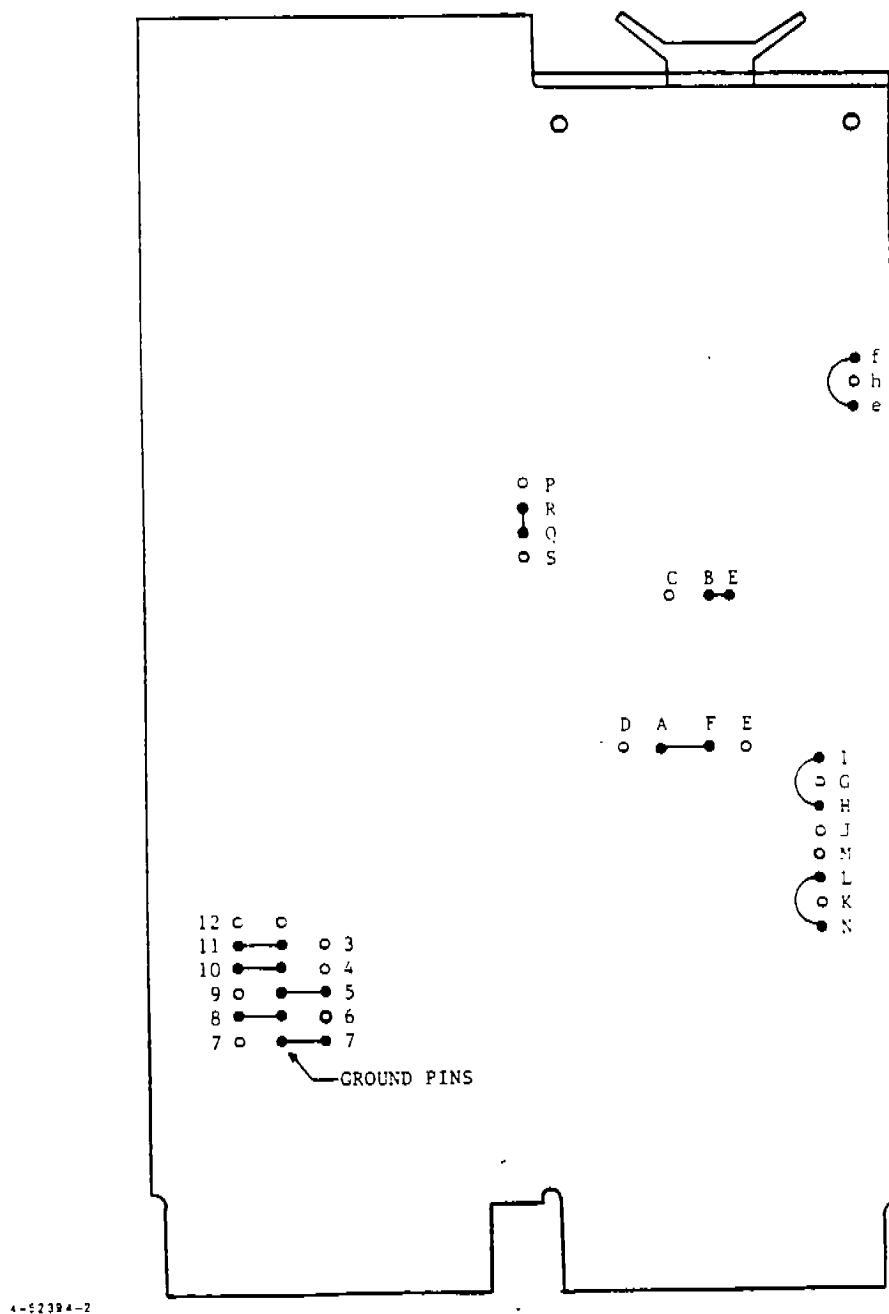
<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
Dual Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test of the DMA-QB assembly.

19.3 OTHER DOCUMENTATION. Other documentation required for testing of the DMA-QB assembly is the DMA-QB Instruction Manual (TI 6490.8).

19.4 PREPARATION FOR TEST. To prepare the DMA-QB assembly for test, follow the instructions listed below:

1. Verify that DMA-QB (unit to be tested) is configured as in one of following figures. Figure 19-1, Figure 19-2 or Figure 19-3.
2. Verify that System Power switch is set to ON position.
3. Turn Electronics Chassis Power switch to OFF position.
4. Remove MADTS system cable P/N 401-37767-01 (W11, P2) from MADTS system DMA-QB in slot A1-U3 of Electronics Chassis card cage.
5. Remove MADTS system DMA-QB from slot A1-U3 of Electronics Chassis card cage.
6. Insert standard DEC dual extender board into slot A1-U3 of Electronics Chassis card cage.



4-52394-2

Figure 19-1. DMA-QB #1 Configuration

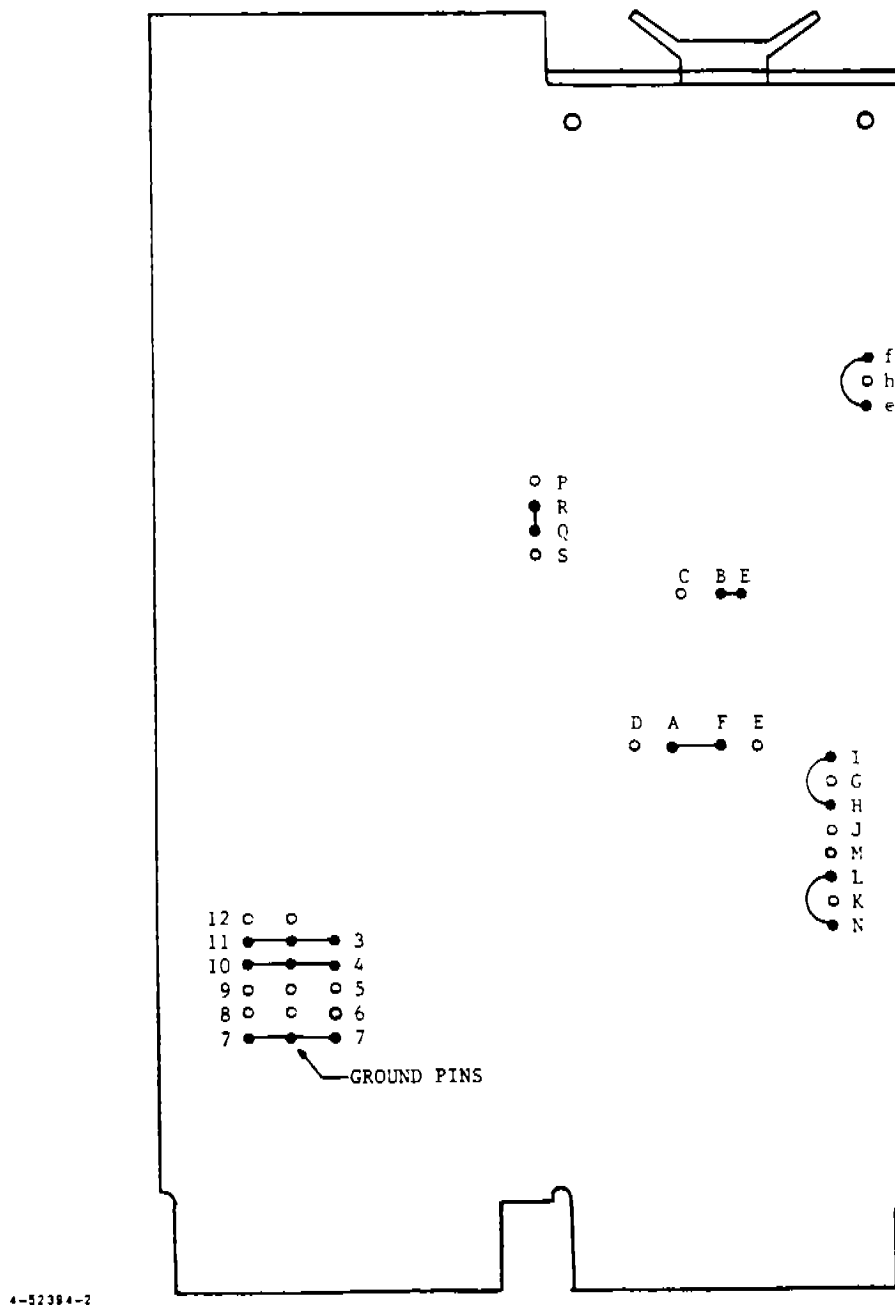


Figure 19-2. DMA-QB #2 Configuration

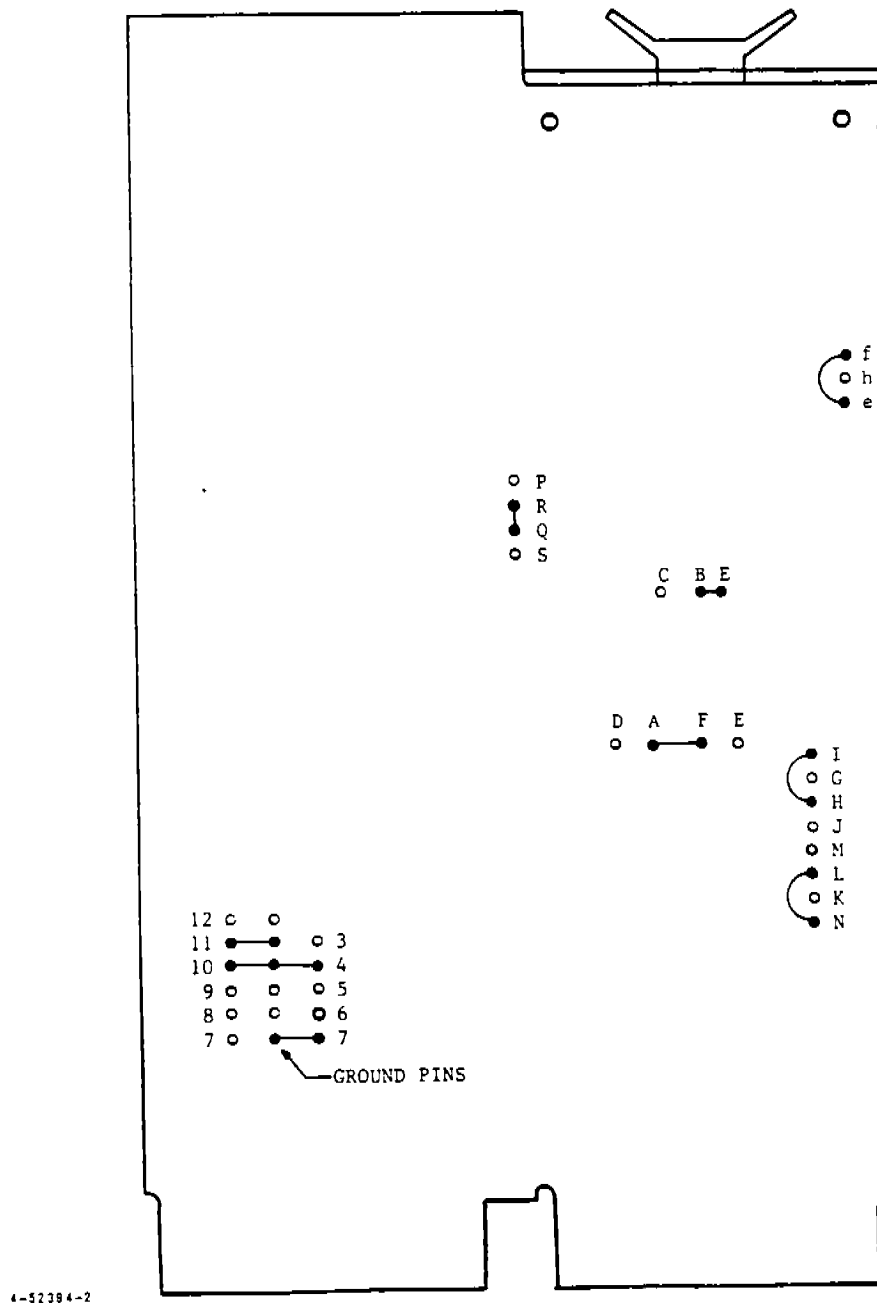


Figure 19-3. DMA-QB #3 Configuration

7. Install DMA-QB (unit under test) into slot A1-U3 of card cage.
8. Install MADTS sytem cable P/N 401-37767-01 (W11, P2) into DMA-QB (unit under test) in slot A1-U3 of card cage.
9. As determined in step 1, if DMA-QB is configured as in Figure 19-1, proceed to paragraph 19.6. If DMA-QB is configured as in Figure 19-2, proceed to paragraph 19.7, or if configured as in Figure 19-3, then proceed to paragraph 19.8.

19.5 DMA-QB #1 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

?

@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

KT *
KP *
MP *.....
MR
MS **.....
RL *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>*SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

KT *
AN????****
CI .
DL*****
FP *
IP *..
KB *
KP *
LA *
LP *
MP *.....
MR*...
MS **.....
MX ***.....
RL *???....
TA .
TK .

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D IP (CR)

Printer response:

IPDIAG:

2. Input: S SU=0+EU=0 (CR)

Printer response:

IPDIAG:

3. Input: X (CR)

Printer response:

X.

00[CSR CWR CPB INR XCS INT ENT DMA DME DMN]

IPDIAG:

4. The DMA-QB #1 configuration diagnostic test is complete. If no errors were reported by MADTS, proceed to paragraph 19.11, the CCA is good.
5. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 19.10 and Table 19-1, DMA-QB/HEX-IPB diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the DMA-QB Instruction Book (TI 6490.8) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty components.
6. Proceed to paragraph 19.9 for Power Down Sequence.

19.6 DMA-QB #2 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with an initial message. A typical message is shown in paragraph 19.6.

The MADTS is now ready to begin testing.

1. Input: D IP (CR)

Printer response:

IPDIAG:

2. Input: S SU=1+EU=1 (CR)

Printer response:

IPDIAG:

3. Input: X (CR)

Printer response:

X.

01[CSR CWR CPB INR XCS INT ENT DMA DME DMN]

IPDIAG:

4. The DMA-QB #2 configuration diagnostic test is complete. If no errors were reported by MADTS, proceed to paragraph 19.11, the CCA is good.
5. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 19.10 and Table 19-1, DMA-QB/HEX-IPB diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the DMA-QB Instruction Book (TI 6490.8) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty components.
6. Proceed to paragraph 19.9 for Power Down Sequence.

19.7 DMA-QB #3 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with an initial message. A typical message is shown in paragraph 19.6.

The MADTS is now ready to begin testing.

1. Input: D IP (CR)

Printer response:

IPDIAG:

2. Input: S SU=2+EU=2 (CR)

Printer response:

IPDIAG:

3. Input: X (CR)

Printer response:

X.

02[CSR CWR CPB INR XCS INT ENT DMA DME DMN]

IPDIAG:

4. The DMA-QB #3 configuration diagnostic test is complete. If no errors were reported by MADTS, proceed to paragraph 19.11, the CCA is good.
5. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 19.10 and Table 19-1, DMA-QB/HEX-IPB diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the DMA-QB Instruction Book (TI 6490.8) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty components.

19.8 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove MADTS system cable P/N 401-37767-01 (W12, P2) from DMA-QB (unit under test) in slot A1-U3 of Electronics Chassis card cage.
4. Remove DMA-QB (unit under test) from slot A1-U3 of Electronics Chassis card cage.
5. If additional DMA-QB boards are to be tested, return to paragraph 19.4 and proceed.
6. Remove standard DEC dual extender board from slot A1-U3 of Electronics Chassis card cage.
7. Install MADTS system DMA-QB board into slot A1-U3 of Electronics Chassis card cage.
8. Install MADTS system cable P/N 401-37767-01 (W12, P2) into MADTS system DMA-QB in slot A1-U3 in Electronics Chassis card cage.

19.9 MADTS DMA-Q/HEX-IPB DIAGNOSTIC PROGRAM.

TYPE : QBUS DMA #N
PART NUMBER : DMA-QB

I.D. : Q-BUS DMA #N

TYPE : HEX-L11
PART NUMBER : HEX L-11

I.D. : HEX-L11

TYPE : IPB-11
PART NUMBER : IPB-11

I.D. : INTER-PROCESSOR BUFFER

19.9.1 Calling Sequence.

DEVICE: IP
PROGRAM: DIAG

19.9.2 Function Mnemonics. The test function mnemonics used by the DMA-Q/IPB-HEX diagnostic program are as follows. Unless otherwise noted, functions are enabled by default for the manual test mode and disabled during the automatic test mode.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. CHP	Allows the selection of the HEX board part to be used. Disabled by default.
b. CSR	Ensures that the eight CSRs associated with the board pair can be successfully read. Enabled during the automatic test phase.
c. CWR	Ensures that the eight CSRs associated with the board pair can be successfully written to. Enabled during the automatic test phase.
d. CPB	Ensures that data written into any one CSR does alter the complemented data in the other seven CSRs. Enabled during the automatic test phase.
e. INR	Ensures that a bus reset clears the correct bits in the IBC, IMA, and ICS registers. Enabled during the automatic test phase.
f. XCS	Ensures that all bits of the XCS register are working correctly. Enabled during the automatic test phase.
g. INT	Tests the internal interrupt capability of the DMA-Q. Enabled during the automatic test phase.
h. ENT	Tests the external interrupt capability of the DMA-Q. Enabled during the automatic test phase.
i. DMA	Tests the DMA transfer capability of two DMA-Q boards using nonextended memory. Enabled during the automatic test phase.
j. DME	Tests the DMA transfer capability of two DMA-Q boards using extended memory. Enabled during the automatic test phase.
k. DMN	Tests the error detection capability of DMA-Q boards by using nonexistent memory at one end of a DMA transfer. Enabled during the automatic test phase.

19.9.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error within a stimulus causes error information to be output to the console. The

diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 19-1. The address and contents of a CSR is normally given in the Bit Field Decomposition format, denoted by [BFD]. This diagnostic requires a test DMA-Q board to be connected as the host to an HEX-IPB board pair. The MADTS DMA-Q is connected to the HEX board as a satellite.

19.9.4 Error Output.

Error codes and any associated data are output in the form:

```
ERROR #xxxx      aaaaaa
```

where:

```
xxxx      is the error number
aaaaaa    is an output parameter
```

The number of output parameters will vary from 0 to 1 depending on the error. Additional error data may be given in an automated dump format as follows:

TRANSMIT BUFFER

```
  ADDR  DATA
000000 000001 001004 004020 020100 100377 000301 000310 000320
000020 000001 000002 000003 000004 000005 000006 000007 000010
000040 000010 000012 000013 000014 000015 000016 000017 000020
```

RECEIVE BUFFER

```
  ADDR  DATA
000000 000000 001004 004020 020100 100376 000007 000007 000007
000020 000001 000002 000003 000004 000005 000006 000007 000010
000040 000010 000012 000013 000014 000015 000016 000017 000020
```

The error codes used by the MADTS DMA-Q/HEX-IPB diagnostic program and their associated output parameters are given in Table 19-1.

NOTE

All errors except error #0 will also produce a register dump in the BFD.

A transfer direction value of 1 indicates that the data transfer was from the HEX-Q to the MADTS DMA-Q.

A transfer direction value of 0 indicates that the data transfer was from the MADTS DMA-Q to the HEX-Q.

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CHP	Change port number	The specialist is asked to input the port number to be used for the next pass. The number must be 1 to 6 inclusive. The number that is entered is verified and echoed. The specialist may then connect the DMA interface cable to the desired port before typing the "P" character to proceed with the diagnostic.	none	Invalid part number entered.	
CSR	Read CSR register	Each of the 8 control status registers is read. A check for a bus time-out is performed after each read.	0	Bus time-out error on CSR read.	CSR address
CWR	Write to mailbox registers	For each of the 4 test DMA-QB mailbox registers, a word value of 177777 is written. The data is then read from the corresponding MADTS mailbox register and looped back by writing	2	Bus time-out error on CSR write.	CSR Address CSR contents (BFD)
			4	Cannot set register bits in the CSR.	CSR contents (BFD) CSR Address

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CWR (cont'd)		it back to the MADTS DMA-Q mailbox register. The mailbox register is then checked in order to verify the value.			
	Write to control/status register	For each of the 4 test DMA-QB control/status registers, all read/write bits are written. The registers are read back and verified to ensure that all read/write bits were set.	2	Bus time-out error on CSR write.	CSR Address CSR contents (BFD)
			4	Cannot set register bits in the CSR.	CSR contents (BFD) CSR Address
CPB	Mailbox test # 1	A value of 125252 is written to the mailbox register under test. The complement is written to all other registers, with provision made to protect the unit select bits in the XCS register. Each MADTS mailbox register is read and written in order to loop back the data. The register under test is checked to insure that its contents were not altered.	6	A value of 125252 was written to a CSR but was altered when other CSR's were written with the complement.	CSR address CSR contents

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CPB (cont'd)	Mailbox test # 2	A value of 52525 is written to the mailbox register under test. The complement is written to all other registers, with provision made for protecting the unit select bits of the XCS register. Each MADTS mailbox register is read and written in order to loop back the data. The register under test is checked to insure that its contents were not altered.	8	A value of 52525 was written to a CSR but was altered when other CSRs were written with the complement.	CSR address CSR content
	Control/status test # 1	A value of 125252 is written to the control/status register under test. The complement is written to all other registers, with provision made for protecting the unit select bits of the XCS register as well as setting only the write bits in each of the control/status registers. The register under test is checked to insure that its contents were not altered.	6	A value of 125252 was written to a CSR but was altered when other CSRs received the complement.	CSR address CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CPB (cont'd)	Control/ status test # 2	A value of 52525 is written to the control/status register under test. The complement is written to all other registers, with provision made for protecting the unit select bits of the XCS register as well as setting only the write bits in the control/status registers. The register under test is checked to insure that its contents were not altered.	8	A value of 52525 was written to a CSR, but was altered when other CSRs received the complement.	CSR address CSR contents
INR	IBC register test	A value of 177777 is written to the IBC register and a bus reset is performed. The register is then read to verify that it is zero.	10	IBC is not cleared after a bus reset.	CSR content
	IMA register test	A value of 177777 is written to the IMA register and a bus reset is performed. The register is then read to verify that it was not altered.	12	IMA is cleared after a bus reset.	CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
INR (cont'd)	ICS register test	The MADTS DMA-QB is selected as the slave and its ICS register is cleared. A 177777 is written to the TEST DMA-QB ICS Register. After a bus reset is performed, the register is tested to insure that only the low order 6 bits remain set.	14	Incorrect bits were cleared in the ICS after a bus reset was performed.	CSR content
XCS	Reset XCS test	A value of 77 is moved to the XCS register to reset the satellite flags and clear the other bits.	16	All bits in the XCS cannot be cleared.	CSR content
	XCS bits 7-10 test	each XCS bits 7 through 10 are set and verified.	18	An XCS bit cannot be set.	Bit position CSR content
	XCS host flag bits test	Bits 11-13 in the test DMA-QB are one at a time set and verified. The setting of each bit should cause a corresponding bit in the MADTS DMA-QB to be set. The setting of these bits is verified.	18	An XCS bit cannot be set.	Bit position CSR content
	XCS HGO bit test	Bit 14 in the test DMA-QB is set and verified. The setting of each bit should	18	An XCS bit cannot be set.	Bit position CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
XCS (cont'd)		cause bit 6 in the MADTS DMA-QB to be set. The bit setting is verified.			
	XCS INT bit test	Bit 15 in the test DMA-QB is set and verified. The setting of each bit should cause bit 7 in the MADTS DMA-QB to be set. The bit setting is verified.	18	An XCS bit cannot be set.	Bit position CSR content
	XCS satellite bits test	Bits 8-13 in the MADTS DMA-QB are one at a time set and verified. The setting of each bit should cause a corresponding bit in the test DMA-Q to be set. The setting of these bits is verified.	18	An XCS bit cannot be set.	Bit position CSR content
INT	Clear IBC test	The test IBC is cleared. No interrupt should occur.	20	An internal interrupt occurred when the IBC was cleared.	CSR content
	Internal Interrupt test	A value of 177777 is written to the IBC register to inhibit further data transfers. The internal interrupt request flag in the ICS should be	22	The internal interrupt flag was not set when the IBC was loaded with 177777.	CSR content
			24	An internal inter-	

Table 19-1. DMAQ/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
INT (cont'd)		set. No interrupts should occur. Internal interrupts are then enabled causing only one internal interrupt.		rupt occurred before enable and after the IBC was loaded with 177777.	
			26	An expected internal interrupt did not occur with internal interrupts enabled.	CSR content
			28	More than one internal interrupt occurred with internal interrupts enabled.	CSR content
ENT	Aux request bit test	The MADTS DMA-QB auxiliary request bit is set, which causes the internal interrupt request flag in the test DMA-QB to be set. No interrupts should be generated.	30	Test DMA-QB interrupt request flag not set.	CSR content
			32	An external interrupt occurred.	CSR content
	Enable external interrupt test	The test DMA-QB external interrupt bit is set, which causes an external interrupt to occur. No additional interrupts should be generated.	34	An expected external interrupt did not occur.	CSR content
			36	More than one external interrupt occurred.	CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ENT (cont'd)	External interrupt request bit test	The test DMA-QB interrupt request bit is set, which causes the external interrupt flag in the MADTS DMA-Q to be set.	38	MADTS DMA-QB interrupt request flag was not set.	CSR content
DMA	Forward DMA test	A DMA operation is initiated which transfers a 256 byte buffer from the DMA-QB under test to the MADTS DMA-QB using non-extended memory. Each byte in the buffer contains its relative address. Each DMA-QB will generate an interrupt upon completion of its data transfer. Each DMA-Q register is then cleared. No more interrupts should be received. Finally, the validity of the receive data is verified.	40	One or both internal interrupts did not occur for a DMA transfer.	Transfer direction (1) CSR content
			42	Too many interrupts occurred for a DMA transfer.	Transfer direction (1) CSR content
			44	Receive data does not match the transmit data after a DMA transfer.	Transfer direction (1) Data transmitted Data received CSR content
			56	A bus time-out occurred during a DMA transfer operation.	Transfer direction (1) CSR content
	Reverse DMA test	A DMA operation is initiated which transfers a 256 byte buffer from the MADTS DMA-QB to the DMA-QB under test using non-extended memory. Each byte in the buffer contains its rel-	40	One or both internal interrupts did not occur for a DMA transfer.	Transfer direction (0) CSR content
			42	Too many interrupts occurred for a DMA transfer.	Transfer direction (0) CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DMA (cont'd)		ative address. Each DMA-Q will generate an interrupt upon completion of its data transfer. Each DMA-QB register is then cleared. No more interrupts should be received. Finally, the validity of the receive data is verified.	44	Receive data does not match the transmit data after a DMA transfer.	Transfer direction (0) Data transmitted Data received CSR content
			56	A bus time-out occurred during a DMA transfer operation.	Transfer direction (0) CSR content
DME	Forward DMA test	A DMA operation is initiated which transfers a 256 byte buffer from the DMA-QB under test to the MADTS DMA-QB using extended memory. Each byte in the buffer contains its relative address. Each DMA-QB will generate an interrupt upon completion of data transfer. Each DMA-QB IBC register is then cleared. No more interrupts should be received. Finally, the validity of the receiver data is verified.	46	One or both internal interrupts did not occur for a DMA transfer using extended memory.	Transfer direction (1) CSR content
			48	Too many interrupts occurred for a DMA transfer using extended memory.	Transfer direction (1) CSR content

Table 19-1. DMA-Q/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DME (cont'd)	Reverse DMA test	A DMA operation is initiated which transfers a 256 byte buffer from the MADTS DMA-QB to the DMA-QB under test using extended memory. Each byte in the buffer contains its relative address. Each DMA-QB will generate an interrupt upon completion of data transfer. Each DMA-Q IBC register is then cleared. No more interrupts should be received. Finally, the validity of the receive data is verified.	50	Receive data does not match the transmit data after a DMA transfer using extended memory.	
			56	A bus time-out occurred during a DMA transfer operation.	Transfer direction (0) CSR content
			40	One or both interrupts did not occur after a DMA transfer.	Transfer direction (0) CSR content
			42	An unexpected interrupt occurred after a DMA transfer.	Transfer direction (0) CSR content
			44	Receive data does not match transmit data.	Transfer direction (0) Receive data Transmit data CSR content
			56	A bus time-out occurred during a DMA transfer operation.	Transfer direction (0) CSR content
			40	One or both interrupts did occur after a DMA transfer.	Transfer direction (1) CSR content

Table 19-1. DMAQ/HEX-IPB Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DMN	Forward DMA test	A DMA operation is initiated which transfers a 256-byte buffer from the DMA-QB under test to the MADTS DMA-QB using non-existent memory.	52	An expected internal interrupt did not occur for a DMA transfer with non-existent memory.	Transfer direction CSR content
			54	The test DMA-QB did not detect non-existent memory.	Transfer direction CSR content
	Reverse DMA test	A DMA operation is initiated which transfers a 256-byte buffer from the MADTS DMA-QB to the DMA-QB under test using non-existent memory.	52	An expected internal interrupt did not occur for a DMA transfer with non-existent memory.	Transfer direction
			54	The test DMA-QB did not detect non-existent memory.	Transfer direction

SECTION XX
LRU TEST PROCEDURES
HEX-L11

20.1 GENERAL. This section contains the test procedures for the HEX-L11 printed wiring assembly, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

20.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the HEX-L11 assembly:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570
DUAL Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for testing of the HEX-L11 assembly.

20.3 OTHER DOCUMENTATION. Other documentation required for testing of the HEX-L11 is the HEX-IPB Instruction Book (TI 6490.8).

20.4 PREPARATION FOR TEST. To prepare the HEX-L11 assembly for test, follow the instructions listed below.

1. Verify that System Power switch is set to ON position.
2. Set Electronics Chassis Power switch to OFF position.
3. Disconnect MADTS system cable P/N 401-37767-01 (W12, P1) from the 40-pin connector on the MADTS system HEX-L11 in slot A1-U2 of Electronics Chassis card cage.
4. Remove MADTS system HEX-L11 from slots A1-U1 and A1-U2 of Electronics Chassis card cage and replace with two standard DEC dual extender boards, oriented correctly with respect to key.
5. Disconnect MADTS system cable P/N 401-37767-01 (W11, P1) from port 1 on MADTS system HEX-L11.
6. Install HEX-L11 (unit under test) into two standard DEC dual extender boards.
7. Insert MADTS system cable P/N 401-37767-01 (W11, P1) into port 1 on HEX-L11 (unit under test).

8. Insert MADTS system cable P/N 401-37767-01 (W12, P1) into 40-pin connector in slot A1-U2 on HEX-L11 (unit under test).

20.5 TEST PROCEDURE When the power switch in the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

```

?
@
SELFTEST I CPU RAM REF PAT ADR INT CPY XFR J
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
                *
                *
                *
                *.....
                .....*...
                **.....
                *???.
                0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123

```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
 DFX SYSTEM LOAD UTILITY
 <133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```

MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
                *
                *
                AN .....????****
                CI .
                DL .....*****
                FP *
                IP *..
                KB *
                KP *
                LA *
                LP *
                MP *.....
                MR .....*...
                MS **.....
                MX ****.
                RL *???.
                TA .
                TK .
                0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123

```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D IP (CR)

Printer response:

IPDIAG:

2. Input: S EU=0+CHP (CR)

Printer response:

IPDIAG:

3. Input: X (CR)

Printer response:

X.
00[CHP

Enter port number to be used:

4. Input: 1

Printer response:

Port # under test: 1

Press RETURN to Continue

5. Input: (CR)

Printer response:

CSR CWR CPB INR XCS INT ENT DMA DME DMN]

IPDIAG:

6. Move MADTS System cable P/N 401-37767-01 from Port 1
to Port 2.

7. Input: X (CR)
Printer response:
X.
00[CHP
Enter port number to be used:
8. Input: 2
Printer response:
Port # under test: 2
Press RETURN to Continue
9. Input: (CR)
Printer response:
CSR CWR CPB INR XCS INT ENT DMA DME DMN]
IPDIAG:
10. Move MADTS System cable P/N 401-37767-01 from Port 2 to Port 3.
11. Input: X (CR)
Printer response:
X.
00[CHP
Enter port number to be used:
12. Input: 3
Printer response:
Port # under test: 3
Press RETURN to Continue
13. Input: (CR)
Printer response:
CSR CWR CPB INR XCS INT ENT DMA DME DMN]
IPDIAG:

14. Move MADTS System cable P/N 401-37767-01 from Port 3 to Port 4.
15. Input: X (CR)
Printer response:
X.
00[CHP
Enter port number to be used:
16. Input: 4
Printer response:
Port # under test: 4
Press RETURN to Continue
17. Input: (CR)
Printer response:
CSR CWR CPB INT XCS INT ENT DMA DME DMN]
IPDIAG:
18. Move MADTS System cable P/N 401-37767-01 from Port 4 to Port 5.
19. Input: X (CR)
Printer response:
X.
00[CHP
Enter port number to be used:
20. Input: 5
Printer response:
Port # under test: 5
Press RETURN to Continue
21. Input: (CR)
Printer response:
CSR CWR CPB INR XCS INT ENT DMA DME DMN]
IPDIAG:

22. Move MADTS System cable P/N 401-37767-01 from Port 5 to Port 6.
23. Input: X (CR)
Printer response:
X.
00[CHP
Enter port number to be used:
24. Input: 6
Printer response:
Port # under test: 6
Press RETURN to Continue
25. Input: (CR)
Printer response:
CSR CWR CPB INR XCS INT ENT DMA DME DMN]
IPDIAG:
26. The HEX-L11 diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.
27. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 19.7 and Table 19-1 in section 19. HEX-IPB diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic. Refer to the HEX-L11 Instruction Book TI 6490.8 for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

20.6 POWER DOWN PROCEDURE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Disconnect MADTS system cable P/N 401-37767-01, W12, P1 from port 6 on HEX-L11 under test.
4. Disconnect MADTS system cable P/N 401-37767-01 (W11, P1) from 40-pin connector in slot A1-U2 on HEX-L11 under test.

5. Remove HEX-L11 (unit under test) from DEC dual extender boards in slots A1-U1 and A1-U2 in Electronics Chassis card cage.
6. If additional boards are to be tested, return to paragraph 20.4, step 6, and proceed.
7. Remove two DEC dual extender boards from slots A1-U1 and A1-U2 of Electronics Chassis card cage.
8. Insert MADTS System cable P/N 401-37767-01, W12, P1 into port 1 on MADTS System HEX-IPB.
9. Install MADTS System HEX-L11 into slots A1-U1 and A1-U2 of MADTS card cage.
10. Insert MADTS system cable P/N 401-37767-01, W11, P1 into the 40-pin connector on MADTS system HEX-L11 in slot A1-U2.

SECTION XXI
LRU TEST PROCEDURES
MRV11-C

21.1 GENERAL. This section contains the test procedures for the MRV11-C Circuit Card assembly as tested on the MADTS. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

21.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the MRV11-C assembly:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570
Standard Dual Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test of the MRV11-C assembly.

21.3 OTHER DOCUMENTATION. Other documentation required for testing of the MRV11-C assembly is the MRV11-C Instruction Book (TI 6490.4).

21.4 PREPARATION FOR TEST. To prepare MRV11-C assembly for test, follow the instructions listed below.

1. Inspect and verify that MRV11-C CCA is configured as in Tables 21-1, 21-2, and 21-3. See Figure 21-1.
2. Verify that System Power switch is set to ON position.
3. Set Electronics Chassis Power switch to OFF.
4. Insert standard dual extender board into slot A3-L1 in Electronics Chassis card cage so that it is oriented correctly with respect to its key.
5. Attach jumper from J88 to J89 on MRV11-C (unit under test).
6. Insert MRV11-C (unit under test) into dual extender board in slot A3-L1 so that it is oriented correctly with respect to its key. Do not remove MADTS System MRV11-C.
7. Set Electronics Chassis Power switch to ON position.

Table 21-1. 32k Word PROM MRV11-C Wirewrap Connections

Note: All addresses are in Octal.

J69-J71	Installed	Enable Low-byte MUX		
		Low byte Selection		
J27-J26	Installed	CSR 0	}	Window "0" page number
J30-J29	"	CSR 1		
J33-J32	"	CSR 2		
J36-J35	"	CSR 3		
J39-J38	"	CSR 4		
		High byte Selection		
J9-J8	Installed	CSR 8	}	Window "1" page number
J11-J10	"	CSR 9		
J13-J12	"	CSR 10		
J15-J14	"	CSR 11		
J17-J16	"	CSR 12		
		Prom Window Starting Address		
J47-J48	Installed	Bit 16	}	Window starting address 160000
J49-J50	"	Bit 17		
J51-J52	"	Bit 12		
J86-J87	Installed	Chip Set 0	}	Chip Enable Jumpers
J84-J85	"	Chip Set 1		
J82-J83	"	Chip Set 2		
J80-J81	"	Chip Set 3		
J78-J79	"	Chip Set 4		
J76-J77	"	Chip Set 5		
J74-J75	"	Chip Set 6		
J72-J73	"	Chip Set 7		
J92-J93	Removed	Bit 1	}	CSR Address *77000
J94-J95	"	Bit 2		
J96-J97	"	Bit 3		
J90-J91	"	Bit 4		

* Bank 7 asserted (1 for 32K words - 7 for 128K word systems)

Table 21-1. 32k Word PROM MRV11-C Wirewrap Connections (Continued)

J88-J89	Removed	Enable Bootstrap
J18-J16	Installed	Starting Address 3000
J19-J20	"	in page 31 (Fourth 512 byte's of
J20-J21	"	chip set 0.)
J21-J22	"	
J22-J24	"	
J67-J68	Installed	Bit 15 Disable Module Enable
A12	J115-J114 and J118-J119	U43, 44
	J121-J122	U37, 38
	J124-J125	U31, 32
	J127-J128	U25, 26
	J101-J102	U41, 42
	J98-J99	U35, 36
	J104-J105	U29, 30
	J107-J108	U23, 24
A11	J113-J112	
+5 VDC	J117-116	
	J2-J3	200-450 nsec Chip Access Time

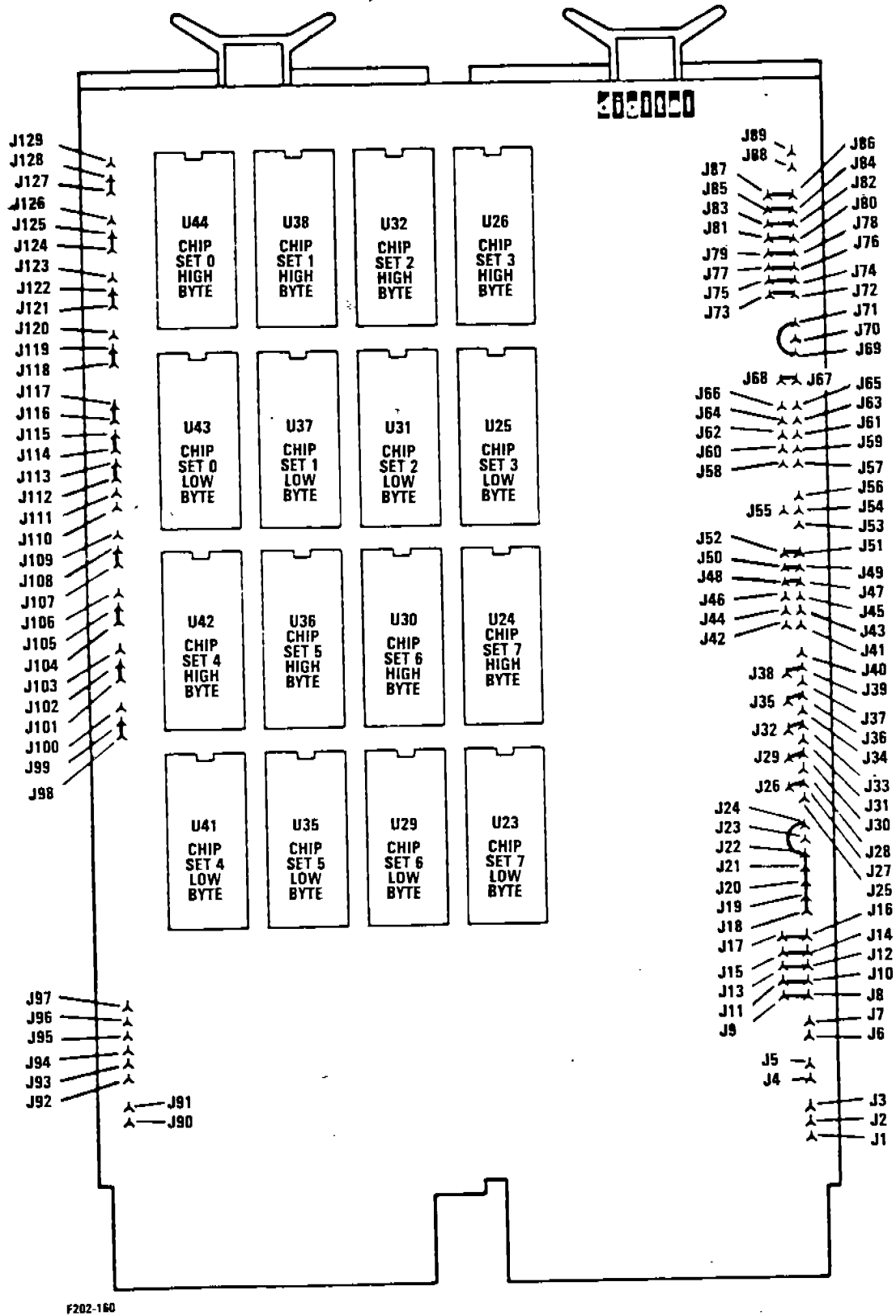


Figure 21-1. MRV11-C Wirewrap Pin Location

Table 21-2. 32k Word PROM MRV11-C Part Numbers

COMMUNICATION PROCESSOR

<u>ESY</u>	<u>P/N</u>	<u>SET NUMBER</u>	<u>LOCATION</u>
316-3044-X		0	U44
316-3045-X		0	U43
316-3046-X		1	U38
316-3047-X		1	U37
316-3048-X		2	U32
316-3049-X		2	U31
316-3050-X		3	U26
316-3051-X		3	U25
316-3052-X		4	U42
316-3053-X		4	U41
316-3054-X		5	U36
316-3055-X		5	U35
316-3056-X		6	U30
316-3057-X		6	U29
316-3058-X		7	U24
316-3059-X		7	U23

POSITION PROCESSOR

316-3060-X	0	U44
316-3061-X	0	U43
316-3062-X	1	U38
316-3063-X	1	U37
316-3064-X	2	U32
316-3065-X	2	U31
316-3066-X	3	U26
316-3067-X	3	U25
316-3068-X	4	U42
316-3069-X	4	U41
316-3070-X	5	U36
316-3071-X	5	U35
316-3072-X	6	U30
316-3073-X	6	U29
316-3074-X	7	U24
316-3075-X	7	U23

Note: The number of memory devices installed in the locations U23 through U44 may vary as a function of the S/W program. See PROM Set MRV11-C drawing 401-37747 for installation.

Note: -X represents the latest revision.

Table 21-3. 32k Word PROM MRV11-C
System-PROM Address Cross Reference

Note: ;all addresses are in Octal.

<u>System Address - (20,000 *n)</u>	<u>PROM Address</u>	<u>Word #</u>	<u>Byte #</u>
0 - 0776	0000 - 0377	256	512
1000 - 1776	0400 - 0777	512	1024
2000 - 2776	1000 - 1377	768	1536
3000 - 3776	1400 - 1777	1024	2048
4000 - 4776	2000 - 2377	1280	2560
5000 - 5776	2400 - 2777	1536	3072
6000 - 6776	3000 - 3377	1792	3584
7000 - 7776	3400 - 3777	2048	4096
10000 - 10776	4000 - 4377	2304	4608
11000 - 11776	4400 - 4777	2560	5120
12000 - 12776	5000 - 5377	2816	5632
13000 - 13776	5400 - 5777	3072	6144
14000 - 14776	6000 - 6377	3328	6656
15000 - 15776	6400 - 6777	3584	7168
16000 - 16776	7000 - 7377	3840	7680
17000 - 17776	7400 - 7777	4096	8192

n = chip set #

21.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                01234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....*
MR              *.....*
MS              **.....
RL              *???.

                0.....1.....2.....3.....4.....5.....6...
                01234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                01234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....*
MR              *.....*
MS              **.....
MX              ****.
RL              *???.
TA              .
TK              .

                0.....1.....2.....3.....4.....5.....6...
                01234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MR (CR)

Printer response:

MRDIAG:

2. Input: X (CR)

Printer response:

X.

00[CSR WIN SUM

Set0 HL	Set1 HL	Set2 HL	Set3 HL	Set4 HL	Set5 HL	Set6 HL	Set7 HL
****	****	****	****	****	****	****	****
****	****	****	****	****	****	****	****

*The numbers printed are checksums of the PROMs in the unit under test. Therefore, these numbers will depend upon which PROMs are installed in the board. Check the 316-XXXX drawings for the correct checksums. Refer to Table 21-2 to identify location and set number. For every empty socket, the checksum should be F000.

NOTE

Some MRV11-C boards may yield unpredictable data values from unpopulated sockets. It may be necessary to populate all PROM sockets prior to testing.

NOTE

In the event that the device under test is a Model 1 board, an appropriate message will be output to the console.

4. The MRV11-C diagnostic test is complete. If no errors were reported by MADTS, the CCA is good.
5. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 21.7 and Table 21-4, MRV11-C diagnostic error message description. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the MRV11-C Instruction Book (TI 6490.4) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

21.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove MRV11-C CCA under test from standard DEC dual extender board.
4. If additional MRV11-C CCA is to be tested, return to paragraph 21.4 and proceed.
5. Remove standard DEC dual extender board from slot A3-L1 in Electronics Chassis card cage.

21.7 MADTS DEC MRV11-C PROM DIAGNOSTIC PROGRAM.

TYPE: 32KW PROM
PART NUMBER: MRV11-C

I.D.: 32 KWORD PROM MEMORY
CONFIGURE PER SPEC: 406-02152

21.7.1 Calling Sequence.

Device: MR
Program: DIAG

21.7.2 Function Mnemonics. The test function mnemonics used by the parity device diagnostic program are as follows:

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. CSR	Tests CSR.
b. WIN	Verifies window functions by testing map-in ability, response on bus, and checking page content.
c. SUM	Performs ROM content verification.
d. BOT	Performs bootstrap verification.

21.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation is applied causes error information to be output to the console. The

diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 21-4.

21.7.4 Error Output.

Error codes and any associated data are output in the form:

```
ERROR # xxxx      aaaa      bbbb
```

where:

```
xxxx  is the error number
aaaa  is the first parameter (Expected data)
bbbb  is the second parameter (Actual data)
```

The number of output parameters can vary from zero to two depending on the error (two for CSR error, and zero for other errors).

For the SUM function, additional output is given in the MADTS Annotated Dump format. The data displayed is the checksum computed for each set of PROM chips in the MRV11-C module. The data are displayed in hexadecimal for comparison with the original PROM. The display format is shown as follows:

```
Set0 HL  Set1 HL  Set2 HL  Set3 HL  Set4 HL  Set5 HL

wwwwww   wwwwww   wwwwww   wwwwww   wwwwww   wwwwww
zzzzzz   zzzzzz   zzzzzz   zzzzzz   zzzzzz   zzzzzz

Set6 HL  Set7 HL

wwwwww   wwwwww
zzzzzz   zzzzzz
```

where:

wwwwww is the checksum for the high-order PROM chip of the set

zzzzzz is the checksum for the low-order PROM chip of the set.

The error code used by the MADTS MRV11-C PROM module diagnostic and their associated output parameters are given in Table 21-4.

Table 21-4. MRV11-C Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CSR	CSR1: Response On Bus	The CSR stimulus attempts to access the device CSR (checking for response), and declares a bus error if it cannot.	0	Bus error(s) occurred	None
	CSR2: Set/Clear Bits	The CSR2 stimulus verifies that all read/write bits of the CSR can be set and cleared. It first tries to set only the window disable bit, reads the CSR and verifies that the bit was set. The stimulus then performs a loop in which it writes a bit pattern to the 'window 0' bits, reads the CSR, and verifies that the pattern was written correctly. The loop is continued until either an error is detected or all permutations of the bit pattern are used. A similar test is then performed on the "window 1" bits.	2	Incorrect CSR value was detected.	CSR contents (BFD) Expected data Actual data
WIN	WIN 1: Test Memory Windows	The stimulus sets up a loop to map-in each 1 KW page via high- and low-order address windows.	2	Incorrect CSR value was detected.	CSR contents (BFD) Expected data Actual data

Table 21-4. MRV11-C Diagnostic Error Message Description (Cont'd)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		Within this loop, the stimulus performs the following testing: 1) the stimulus attempts to select the desired 1 KW page by setting bits in the CSR. It checks for 'CSR' errors that may occur, 2) WIN1 sets up a loop to access all locations of the current page, via the low-order window. It counts the number of bus errors that occur, and declares both partial (some bus errors) and total (all locations gave bus errors) failures, 3) WIN1 performs the same testing, via the high-order address window, as done in '2', and 4) WIN1 sets up a loop to compare the contents of each location mapped-in via the low-order address window to the contents mapped-in via the high-order window (should be the same). The stimulus declares a comparison error if the windows do not show identical page data.	4	Unable to access any 'page' locations when using the high-order address window.	CSR contents (BFD)
			6	Unable to access some 'page' locations when using the high-order address window.	CSR contents (BFD)
			8	Unable to address any page locations when using the low-order address window.	CSR contents (BFD)
			10	Unable to access some 'page' locations when using the low-order address window.	CSR contents (BFD)
			12	Windows do not show identical 'page' data, when accessing the same page via both windows.	CSR contents (BFD)

Table 21-4. MRV11-C Diagnostic Error Message Description (Cont'd)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SUM	SUM 1: Compute CRC For Chips	The SUM stimulus utilizes the low- and high-order address windows to compute the checksum of every chip. The stimulus first attempts to map-in the appropriate 'pages' by setting bits in the CSR, and checking for CSR errors. Then for each of the 8 sets of PROM chips (one high-order and one low-order chip per set), the stimulus computes the checksum for the 'high-order' chip and the checksum for the 'low-order' chip. SUM saves the checksum data in a table, which it displays in annotated dump format at the end of the function.	2	Incorrect CSR value was detected.	CSR contents (BFD) Expected value Actual value At the end of this function, CRC data is displayed for each PROM chip.

Table 21-4. MRV11-C Diagnostic Error Message Description (Cont'd)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
BOT	BOT 1: Compare Bootstrap Areas	The BOT1 stimulus first attempts to clear the 'disable' bit in the CSR in order to allow it to map-in pages of PROM. It checks for, and reports, 'CSR' errors. The stimulus then executes a loop to compare all words in the I/O page bootstrap area to all words in PROM bootstrap area. BOT1 checks for bus errors and bootstrap mismatch errors that might occur during the comparison.	0	Bus error occurred.	None
			2	Incorrect CSR value was detected.	CSR content (BFD) Expected data Actual data
			14	Word in J/O page bootstrap area did not match corresponding word in PROM bootstrap area.	None

SECTION XXII
LRU TEST PROCEDURES
MSV11-LF

22.1 GENERAL. This section contains test procedures for the MSV11-LF Circuit Card Assembly as tested on the MADTS. The test is conducted under software control which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

22.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the MSV11-LF assembly:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
Standard Dual Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test of the MSV11-LF assembly.

22.3 OTHER DOCUMENTATION. Other documentation required for testing of the MSV11-LF assembly is the MSV11-LF Instruction Book (TI 6490.4).

22.4 PREPARATION FOR TEST. To prepare the MSV11-LF assembly for test, follow the instructions listed below:

1. Verify that System Power switch is set to ON position.
2. Set Electronics Chassis Power switch to OFF.
3. Remove MADTS system MSV11-LF CCA from slot A1-L2 in Electronics Chassis card cage.
4. Insert standard DEC dual board extender into slot A1-L2 in Electronics Chassis card cage so that it is oriented correctly with respect to its key.
5. Insert MSV11-LF CCA under test into standard DEC dual extender board.

22.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

2-
@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
KD *
KT *
KP *
MP *.....
MR*...
MS **.....
RL *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>*SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

MADTS::V00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
KD *
KT *
AN????****
CI .
DL*****
FP *
IP *..
KB *
KP *
LA *
LP *
MP *.....
MR*...
MS **.....
MX ***....
RL *???....
TA .
TK .

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MS (CR)

Printer response:

MSDIAG:

NOTE

Program execution time required in step 3 is approximately 15 minutes.

2. Input: X (CR)

*Printer response:

X.

00 [MAP IOC DAT PAR WRD PAT REF]

MSDIAG:

3. Input: (ESC)

Printer response:

\$

MS :

4. Input: (ESC)

Printer response:

\$

:

5. Input: D MP (CR)

Printer response:

MPDIAG:

6. Input: X (CR)

Printer response:

X.
00[CSR PAR]

MPDIAG:

7. The MSV11-LF 64K word RAM CCA diagnostic test is complete. If no errors are reported by MADTS, the assembly is good.
8. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 22.7 and Table 22-1, MSV11-LF Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the MSV11-LF Instruction Book (TI 6490.4) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

22.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove DEC MSV11-LF 64K Word RAM CCA (unit under test) from dual board extender.
4. If additional MSV11-LF CCAs are to be tested return to paragraph 22.4, step 5 and repeat test with next MSV11-LF CCA. Otherwise, continue Power Down Sequence.
5. Remove dual extender board from slot A1-L2 of Electronics Card cage.
6. Insert MADTS System MSV11-LF CCA into slot A1-L2 of Electronics Card Cage.

22.7 MADTS DEC MS11 RAM (22-BIT) DIAGNOSTIC PROGRAM.

TYPE : 64KW RAM I. D. : 64 KWORD RAM MEMORY
 PART NUMBER : MSV11-LF CONFIGURE PER SPEC : 406-02151

22.7.1 Calling Sequence

Device: MS
 Program: DIAG

22.7.2 Function Mnemonics

The test function mnemonics used by the MS11 RAM diagnostic program are described as follows:

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Functions</u>
a. MAP	Creates a bit map which describes the organization of RAM for the system. (Map used by other functions.)
b. IOC	Tests and exercises circuitry responsible for bus protocol, high-order address, address decode, read-write data, parity, RAM refresh and refresh arbitration.
c. DAT	Tests and exercises all RAM cells using worst-case bit patterns.
d. PAR	Tests parity bits throughout addressing space with worst-case bit patterns.
e. WRD	Performs unique-addressing tests, on each word of RAM memory.
f. PAT	Tests/exercises all RAM utilizing a worst-case data noise pattern (parity is disabled).
g. REF	Tests and exercises the refresh capability of RAM.
h. DIN	Performs a pure DATI bus cycle, against the specified range of addresses.
i. DOT	Performs a DATO bus cycle against a specified range of addresses.
j. DIO	Performs a DATIO bus cycle against a specified range of addresses.

22.7.3 Function Stimuli Descriptions

A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation is applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimuli for each function and associated error data is given in Table 22-1.

- NOTES:
1. There must exist at least 1 fully functional bank of 32KW RAM for this diagnostic to work. Internal variables are adjusted according to the size of installed memory; memory is cleared during the auto-phase, which must run to completion for the memory clear to be complete.
 2. If CPU cache is present, it must be disabled for this program to work correctly (assumed already disabled by monitor)
 3. Where appropriate, error information is accumulated during function execution and then dumped upon completion of function. Option CE (Continue on Error) controls this feature. Option DE (Dump on Error) is required for the dump to occur.
 4. It is assumed that if a unique-addressing conflict occurs encompassing the high-order four address bits (22 total), then the program is running on a small system (18 bit) versus large system (22 bit) and adjustment is automatically made to internal variables.

22.7.4 Error Output

Error codes and any associated data are output in the following form:

```
ERROR #xxxx    aaaa  bbbb  cccc  dddd  eeee  ffff  gggg
```

where:

```
xxxx    is the error number
aaaa-   are the output parameters
gggg
```

For certain stimuli, error information is given in the annotated dump format as shown as follows (with sample data):

Error #	Phase	Vector	Adr Hi	Adr Lo	Expctd	Actual	Sys	Siz
000006		000001	000000	000017	000000	077777	160000	000077
000006		000002	000114	000017	000000	100000	160000	000077

Error #8 (indicates that this is an error dump)

The error codes used by the MADTS MS11 RAM diagnostic program and their associated output parameters are given in Table 22-1.

Table 22-1. MSV11-LF Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC	IOC 0: Response On Bus	This stimulus tests the availability of each 32KW bank, and a bus error is issued if a bank is not available.	0	Bus error was detected.	Phase ID = 0 Trap address 22 bit address Expected data Actual data System size
	IOC 1: Worst-case Patterns	The IOC1 stimulus tests the first location of the current bank, using worst case data patterns. Since the purpose of this function is to test module circuitry, rather than RAM chip integrity, execution against any location in the module will suffice. The stimulus performs a loop in which it writes a data pattern (1 in a 0 field, or 0 in a 1 field) at the current location and checks for data comparison errors, bus errors, and parity trap errors. If the option 'Continue on Error' is not selected, the	0	Bus error was detected.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		stimulus immediately reports any detected errors. If the 'CE' option is selected, the stimulus rotates the pattern and continues testing. After all permutations of the test patterns have been used, the stimulus then executes the annotated dump, which contains the error number, function phase, trap address, 22 bit address (high-order 6 bits), 22 bit address (low-order 16 bits), expected data, actual (read) data, and system size. This data represents error(s) that occurred during the stimulus. These errors are reported only at the end of stimulus since the 'CE' option forced continued testing.	6	Contents of RAM location do not match expected data.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
	IOC 2: Parity Patterns	This stimulus performs parity pattern tests on the first location of each 32KW bank. It utilizes	0	Bus error was detected.	Phase ID = 2 Trap address 22 bit address Expected data

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		a series of worst-case patterns to write to a location, read back data, and check for errors. The stimulus records error information. If the 'CE' option is disabled, the IOC2 stimulus immediately reports detected errors. If 'CE' is selected, the stimulus continues the pattern tests, recording any error information. After testing with all the parity patterns, the stimulus performs an annotated dump (when 'Dump on error' is enabled).	2	Spurious interrupt occurred.	Actual data System size Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
	IOC 3: Test Read- modify Write Cycle	This stimulus tests the read-modify-write cycle in the first location of the current bank. Since read-modify-write (DATIO) cycle uses a unique bus protocol sequence (con-	0	Bus error was detected.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		tinuous assertion of bus control, during both read and write) it is tested independently of other RAM module functions. The IOC3 stimulus clears the first location, and performs a 'complement' operation on the contents of the first location (instruction uses DATIO cycle). The stimulus then takes the resultant value from the location as 'actual' data. It then checks for bus errors and trap errors, and compares expected (all '1's) to actual data. The stimulus reports detected errors.	2	Spurious interrupt occurred.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
	IOC 4: Test Write- byte Cycle	This stimulus tests the 'write-byte' cycle in the first location of the current bank. Since the purpose of this function is to test module circuitry, execution	0	Bus error was detected.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		against any location in the module is sufficient. The stimulus performs 'DATOB' cycles on the low and high bytes, then uses the 'DATI' resultant data as 'actual' data. The stimulus then checks for interface errors, and compares 'actual' to expected data. It then issues detected errors.	2	Spurious interrupt occurred.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error occurred.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
	IOC 5: Test Refresh	This stimulus tests re-fresh and access/refresh arbitration against the first two locations in the current bank. A unique pattern is written into the first location. Then the second location is accessed repeatedly for	0	Bus error was detected.	Phase ID = 5 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 5 Trap address

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		a sufficient period of time to ensure that a refresh or access/refresh arbitration problem will surface as a hard failure or race condition. The stimulus then checks for interface errors, and compares the pattern ('expected' data) to the actual value from the first location. Then any detected error(s) are reported.	4	Parity trap error detected.	22 bit address Expected data Actual data System size Phase ID = 5 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 5 Trap address 22 bit address Expected data Actual data System size
	IOC 6: Unique Addressing	The stimulus performs a unique addressing test against every available 32KW bank. An encoded form of the current bank number is written into first location of current bank. Then encoded bank numbers are written into the first locations of all other available banks in the range 00 thru (current	6	Contents of RAM location do not match expected data.	Phase ID = 6 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IOC (Cont'd)		bank # - 1). Encoded bank #'s are written into first locations of all other available banks in the range (current# +1) thru 77 (octal). The stimulus then reads the first location of current bank and compares it against the expected encoded bank number. It then reports comparison errors.			
DAT	DAT 1: Test Data Cells	This stimulus tests all words throughout address space by writing each permutation of the '0' in '1's field into the current word, reading the word, and noting comparison errors. The stimulus then writes each permutation of '1's in a '0's field, reads the word, and notes comparison errors. If the 'CE' option is disabled, the stimulus reports an error at the first opportunity. If 'CE' is enabled, then the	6	Contents of RAM location do not match expected data.	Phase ID = 0 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DAT (Cont'd)		stimulus records any errors, and continues testing the remaining words. It performs an annotated dump of the error information after all words in address space are tested.			
PAR	PAR 1: Test Parity Bits	This stimulus tests all addressing space using a set of worst-case parity patterns. It writes each pattern to the current location and compares the original pattern to actual (readback) data. The stimulus checks for parity trap errors and other interface errors. If the 'CE' option is disabled, the stimulus reports detected errors at the first opportunity. If 'CE' is enabled, the stimulus records the detected error, and continues testing. After all	0	Bus error was detected.	Phase ID = 0 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 0 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 0 Trap address 22 bit address Expected data

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PAR (Cont'd)		addressing space is tested, the stimulus executes an annotated dump of the error information.	6	Contents of RAM location do not match expected data.	Actual data System size Phase ID = 0 Trap address 22 bit address Expected data Actual data System size
WRD	WRD 1: Normal, Upward Test	This stimulus performs the address uniqueness test, starting at the lower 32KW bank and tests upward. It writes the current location address into that location, compares the readback data to the expected address, and notes data comparison errors. If the 'CE' option is disabled, the stimulus reports any detected errors at the first opportunity. If 'CE' is enabled, then the stimulus records errors and continues testing the remaining words. It	6	Contents of RAM location do not match expected data.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WRD (Cont'd)		performs an annotated dump of the error information after all words in address space are tested.			
	WRD 2: Downward Test	This stimulus continues the address uniqueness test starting at the higher 32KW bank and testing downward. The stimulus reads each location, compares the readback value to the current address, writes the complement of the address value at the current location, and checks for data readback errors. If the 'CE' option is disabled, the stimulus issues an error at the first opportunity. If 'CE' is enabled, then the stimulus records errors (places them in an I/O buffer), and continues testing the remaining locations. It performs an annotated dump of the error information after	6	Contents of RAM location do not match expected data.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WRD (Cont'd)		all words in address space are tested.			
	WRD 3: Upward Comple- ment Test	This stimulus continues the unique addressing test starting from the lower 32KW bank and moving upward. It reads the current location (actual data) and compares it to the complement of the address (expected data). The stimulus then writes the real address value at the current address and checks for write/readback errors. If the 'CE' option is disabled, the stimulus issues an error at the first opportunity. If 'CE' is enabled, then the stimulus records errors (places them in an I/O buffer), and continues testing the remaining locations. It performs an annotated dump of the error information after all words in address space are tested.	6	Contents of RAM location do not match expected data.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WRD (Cont'd)	WRD 4: Downward Normal Test	This stimulus continues the address uniqueness test starting at the higher 32KW bank, testing downward. It reads the current location and compares the contents to the current address value (noting errors). If the 'CE' option is disabled, the stimulus issues an error at the first opportunity. If 'CE' is enabled, then the stimulus records errors (places them in an I/O buffer), and continues testing the remaining words. It performs an annotated dump of the error information after all words in address space are tested.	6	Contents of RAM location do not match expected data.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
PAT	PAT 1: Upward Write '000377'	This stimulus writes the value '000377' into the current location, starting at lowest bank and moving upward. It then checks for write/readback errors, and	6	Contents of RAM location do not match expected data.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PAT (Cont'd)		records them. If 'CE' is disabled, the stimulus reports errors at the first opportunity. If 'CE' is enabled, then the stimulus continues testing the other RAM locations. It performs an annotated dump of the error information after all of RAM is tested (at end of function).			
	PAT 2: Read Downward	This stimulus reads the current location and compares it to '000377' starting at highest bank and moving downward. It then writes the value '177400' at the location, checks for write/readback errors, and records them. If 'CE' is disabled, the stimulus reports errors at the first opportunity. If 'CE' is enabled, the stimulus continues testing the remaining words. It performs an annotated dump of the error information	6	Contents of RAM location do not match expected data.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PAT (Cont'd)		after all of RAM is tested (at end of function).			
	PAT 3: Upward, Read, Verify '177400'	This stimulus reads the current location and compares it to '177400' starting at lowest bank and moving upward. It then writes the value '000377' at the location, checks for write/readback errors, and records them. If 'CE' is disabled, the stimulus reports errors at the first opportunity. If 'CE' is enabled, the stimulus continues testing the remaining words. It performs an annotated dump of the error information after all of RAM is tested (at end of function).	6	Contents of RAM location do not match expected data.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
	PAT 4: Upward, Read and Verify '000377'	This stimulus reads the current location and compares it to '000377', starting at lowest bank and moving upward. It then	6	Contents of RAM locations do not match expected data.	Phase ID = 4 Trap address 22 bit address Expected data Actual data

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PAT (Cont'd)		writes the value '177400' at the location, checks for write/readback errors, and records them. If 'CE' is disabled, the stimulus reports errors at the first opportunity. If 'CE' is enabled, then the stimulus continues testing the remaining words. It performs an annotated dump of the error information after all of RAM is tested (at end of function).			System size
	PAT 5: Downward Read and Verify '177400'	This stimulus reads the current location and compares it to '177400', starting at highest bank and moving downward. It then writes the value '000377' at the location, checks for write/readback errors, and records them. If 'CE' is disabled, the stimulus reports errors at the first opportunity. If 'CE' is enabled, the stimulus	6	Contents of RAM location do not match expected data.	Phase ID = 5 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PAT (Cont'd)		continues testing the remaining words. It performs an annotated dump of the error information after all of RAM is tested (at end of function).			
REF	REF 1: Refresh Pattern Write	This stimulus writes a pattern to every RAM location, (10101...), that promotes data deterioration in 'weak' RAM cells. It then compares expected to actual data, checks for parity trap errors and other interface errors. If the 'CE' option is disabled, the stimulus reports detected errors at the first opportunity. If 'CE' is enabled, the stimulus records the detected error, continues testing, and executes an annotated dump at the end of the function.	0	Bus error was detected.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
REF (Cont'd)	REF 2: Refresh Pattern Read	After waiting 15 seconds, to allow data to deteriorate in 'weak' RAM cells, the REF2 stimulus reads every RAM location. It then compares expected to actual data, checks for parity trap errors and other interface errors. If the 'CE' option is disabled, the stimulus reports detected errors at the first opportunity. If 'CE' is enabled, the stimulus records the detected error, and continues testing. After all of RAM is tested (end of function), the stimulus executes a dump of the accumulated error information.	6	Contents of RAM location do not match expected data.	Phase ID = 1 Trap address 22 bit address Expected data Actual data System size
			0	Bus error was detected.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 2 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM	Phase ID = 2

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
REF (Cont'd)	REF 3: Write Comple- ment Pattern	This stimulus writes a complemented checker-board pattern (010101...) throughout RAM. It then checks for write/readback errors, parity trap errors and other interface errors. If the 'CE' option is disabled, the stimulus reports detected errors at the first opportunity. If 'CE' is enabled, the stimulus records the detected error, continues testing and executes an annotated dump at the end of the function.		location do not match expected data.	Trap address 22 bit address Expected data Actual data System size
			0	Bus error was detected.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 3 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 3 Trap address 22 bit address Expected data Actual data

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
REF (Cont'd)	REF 4: Refresh Pattern Read (Completion)	After waiting 15 seconds, to allow data to deteriorate in 'weak' RAM cells, the REF4 stimulus reads every RAM location. It then compares expected to actual data, checks for parity trap errors and other interface errors. If the 'CE' option is disabled, the stimulus reports detected errors at the first opportunity. If 'CE' is enabled, the stimulus records the detected error, and continues testing. The stimulus executes an annotated dump at the end of the function.	0	Bus error was detected.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
			2	Spurious interrupt occurred.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
			4	Parity trap error detected.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size
			6	Contents of RAM location do not match expected data.	Phase ID = 4 Trap address 22 bit address Expected data Actual data System size

Table 22-1. MSV11-LF Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DIN	DIN1: perform pure 'DATI'	This stimulus performs a 'DATA' cycle for either range specified by the 'SU' and 'EU' options, on the default range (00-77). The stimulus performs a 'DATI' cycle for each address in the appropriate range.		None	
DOT	DOT 1: performs pure 'DATI'	This stimulus performs a 'DATO' cycle for either range specified by the 'SU' and 'EU' options, on the default range (00-76). The stimulus performs a 'DATO' cycle for each address in the appropriate range.		None	
DIO	DIO1: perform DATIO	This stimulus performs a 'DATIO' cycle for the default range, the range specified by 'SU' or 'EU' options.		None	

SECTION XXIII
LRU TEST PROCEDURES
KDF11-AA (M8186)
LSI-11/23 CPU

23.1 GENERAL. This section contains test procedures for the LSI-11/23 CPU assembly, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

23.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the LSI-11/23 CPU assembly:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
Extender Board	DEC P/N W984-00

Tools other than standard shop tools are not required for test of the LSI-11/23 CPU assembly.

23.3 OTHER DOCUMENTATION. Refer to LSI-11/23 Instruction Book (TI 6490.4) for detailed information on the CPU.

23.4 PREPARATION FOR TEST. To prepare the LSI-11/23 CPU for test, follow the instructions listed below:

1. Inspect MMU chip for visual defects.
2. Verify that KDF11-AA (unit under test) is configured in accordance with Table 23-1 and Figure 23-1.
3. Verify that System Power switch is set to ON position.
4. Set Electronics Chassis Power switch to OFF.
5. Remove MADTS system KDF11-AA board from card slot A1-L1 of Electronics Chassis card cage.
6. Insert standard DEC dual extender board in slot A1-L1. Observe correct key polarity so that extender board is oriented correctly with respect to its key.
7. Insert DEC CCA, KDF11-AA, DEC M8186 (unit under test) into extender board in slot A1-L1 of Electronics Chassis card cage.

23.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

2-
8

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                 012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ***....
RL              *???....
TA              .
TK              .

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

Table 23-1. KDF11-AA Configuration

Jumper Configuration

W1	Installed	Factory - Do Not Change
W2	Removed	
W3	Installed	Factory - Do Not Change
W4	Removed	Line Time Clock Enabled
W5	Removed	Power-Up Mode 2
W6	Installed	PC at bootstrap
*W7	Installed	Halt Trap to 10 _g
W8	Installed	PC at 773000
W9	Removed	Alternate Bootstrap Option - Not Used
W10	"	" " " "
W11	"	" " " "
W12	"	" " " "
W13	"	" " " "
W14	"	" " " "
W15	"	" " " "
W16	Installed	Factory - Do Not Change
W17	Installed	Factory - Do Not Change
W18	Installed	Disable Wake-Up Circuit

*NOTE: Install for Operation - Remove for ODT

Power-Up Mode Selection

Mode	Jumpers		Description
	W5	W6	
0	R	R	PC=24, PS=26 (Factory Configured)
1	I	R	ODT Microcode
2	R	I	PC at Bootstrap
3	I	I	microcode Bootstrap Not Implemented

I = Installed

R = Removed

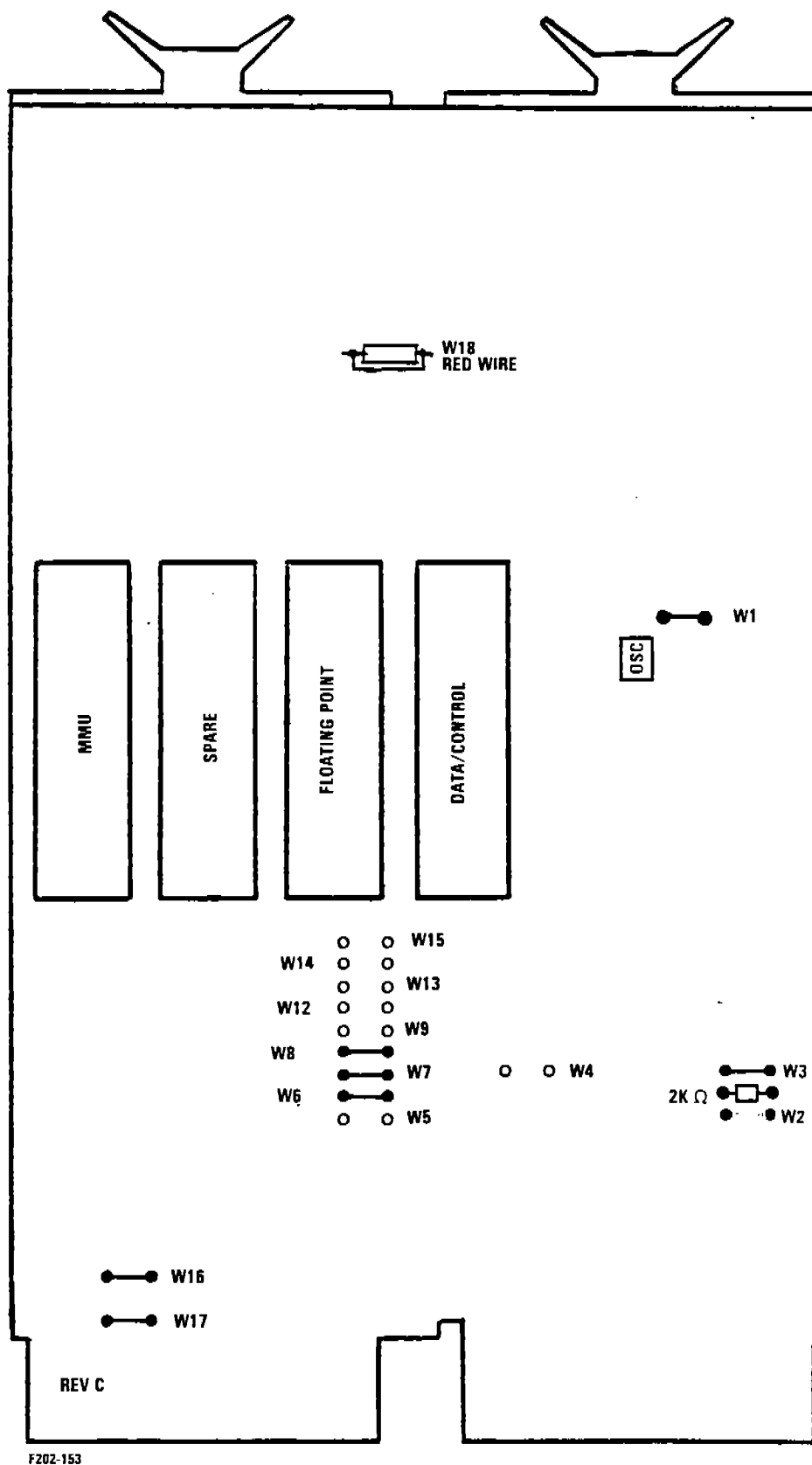


Figure 23-1. KDF11-AA Jumper Locations

The MADTS is now ready to begin testing.

1. Input: D KT (CR)

Printer response:

KTDIAG:

2. Input: X (CR)

Printer response:

X.

00[CPU RAM REF PAT ADR]

KTDIAG:

3. The KDF11 test has ended. Exit by pressing the ESC key.

Input: ESC-Key

Printer response:

\$

KT :

4. Input: ESC-Key

Printer response:

\$

:

Printer response:

KTDIAG:

5. Input: X (CR)

Printer response:

X.

00[PSW REG MAP]

KTDIAG:

6. The MMU test has ended. Exit by pressing the ESC key.

Input: ESC-Key

Printer response:

\$

KT :

7. Input: ESC-Key

Printer response:

\$

:

8. Input: D MP (CR)

Printer response:

MPDIAG :

9. Input: X (CR)

Printer response:

X.

00[CSR PAR]

MPDIAG:

10. The Parity Device test has ended. Exit by pressing the ESC key.

Input: ESC-Key

Printer response:

\$

MP :

11. Input: ESC-Key

Printer response:

\$

:

12. Input: D KP (CR)

Printer response:

KPDIAG:

13. Input: X (CR)

Printer response:

X.

00[BUS BIT CKD CKE INT TIM]

KPDIAG:

14. The KDF11-AA test is complete. If no errors were reported by MADTS, the CCA is good.

15. If an error is detected by the diagnostic, an error message will be generated. To interpret the error message, refer to paragraph 23.7 and Table 23-2, LSI-11/23 Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the LSI-11/23 Processor Instruction Book (TI 6490.4) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

23.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT Position.
2. Set Electronics Chassis Power switch to OFF position.
3. Remove KDF11-AA (unit under test) from dual extender board.
4. If additional KDF11-AA boards are to be tested, return to paragraph 23-4.
5. Remove dual board extender from card slot A1-L1.
6. Insert MADTS system KDF11-AA board into slot A1-L1.

23.7 MADTS DEC KT11 MMU (22-BIT) DIAGNOSTIC PROGRAM.

23.7.1 Calling Sequence.

Device: KT
Program: DIAG

23.7.2 Function Mnemonics. The test function mnemonics used by the KT11 MMU diagnostic program are as follows:

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Functions</u>
-----------------	------------------

- | | |
|--------|--|
| a. PSW | Test the features of the PSW associated with the MMU |
| b. REG | Test every MMU register (CSRs, PARs and PDRs) |
| c. MAP | Test kernel and user mapping |

23.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation has been applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected.

Digital's diagnostic CJKDACO KTF11-AA was used as a reference in designing and coding this diagnostic. No assumptions are made about the provision for SUPERVISOR MODE registers or mapping functionality. The protection features are not exercised, and it is assumed that at least 32kW physical RAM exists and functions correctly. Due to the BLACK BOX nature of the MMU implementation (single LSI chip), it is assumed that upon fault detection, the action taken is to reseal or replace the MMU chip. Therefore no attempt is made to pinpoint faults beyond providing an indication of a general failure mode and isolation of the failure to the MMU device.

The stimuli for each function and associated error data are given in Table 23-2.

NOTE

The KT11 MMU test does not exercise the high-order 6 bits of a 22-bit address.

23.7.4 Error Output.

Error codes and any associated data are output in the form:

```
ERROR #xxxx    aaaa    bbbbbb
```

where:

```
xxxx    is the error number
aaaaaa  is an output parameter
bbbbbb  is an output parameter
```

The error codes used by the MADTS KT11 MMU diagnostic program and their associated output parameters are given in Table 23-2.

23.8 MADTS DEC PARITY DEVICE (22-BIT) DIAGNOSTIC PROGRAM.

23.8.1 Calling Sequence.

```
Device:  MP
Program:  DIAG
```

23.8.2 Function Mnemonics. The test function mnemonics used by the parity device diagnostic program are described below. This program validates the memory size jumper on the RAM board. If the jumper on a small system is set to 22 bits, no error is flagged because no error can result. If the jumper is set to 18 bits on a 22 bit (large) system, an error is flagged because the result is a constrained system.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Functions</u>
a. CSR	Tests response on bus of parity device, and ensures read/write bits of CSR can be cleared and set.
b. PAR	Tests ability of the parity device to generate both correct and incorrect parity, check for correct parity, and trap properly detection of a parity error.

23.8.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation is applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. Digital's 'CZQMCGO 0-124K' diagnostic was used as a reference in designing and coding this diagnostic. The stimuli for each function and associated error data are given in Table 23-2.

NOTE

If CPU Cache is present, it must be disabled in order for this program to work correctly (assumed already disabled by monitor). Memory is cleared during the auto-phase confidence check. Thus it is important to allow the auto-phase to run to completion upon initial boot after power-down.

23.8.4 Error Output.

Error codes and any associated data are output in the form:

ERROR #xxxx aaaa bbbb cccc dddd eeee

where:

xxxx is the error number
 aaaa - eeee are the parameter words

The number of output parameters varies from zero to five, depending on the error number. The error codes used by the MADTS parity error diagnostic and their associated output parameters are given in Table 23-2.

23.9 MADTS KPV11-B DIAGNOSTIC PROGRAM. When running the KP Diagnostic program as required in this procedure, refer to Section 14, paragraph 14.7 and Table 14-1 for error messages.

Table 23-2. LSI 11/23 Diagnostic Error Message Description (MMU)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
PSW	PSW Test (Part One)	Interrupt priority level bits (7:5) are set with a bit pattern, read from the PSW, and compared to the expected value. This process is continued until all possible bit combinations are used.	0	PSW priority or mode bits failed a bit pattern test, or modifying the user mode stack pointer affected the kernel mode stack pointer.	
	(Part Two)	The PSW mode bits are tested in the same manner.	0	PSW priority or mode bits failed a bit pattern test, or modifying the user mode stack pointer affected the kernel mode stack pointer.	
	(Part Three)	The value of the kernel stack pointer is saved. The user mode is then enabled and the user mode stack pointer is modified. Finally, the kernel stack pointer is compared to the saved value.	0	PSW priority or mode bits failed a bit pattern test, or modifying the user mode stack pointer affected the kernel mode stack pointer.	
REG	Test all MMU CSRs	A 'DATO' cycle is executed for each CSR address, and a check is made for bus errors. An attempt is made to clear SR0 and SR3, the registers are read, and data errors are reported.	2	Either a MMU register failed to respond on the bus or a bus error was detected at the end of a stimulus.	

Table 23-2. LSI 11/23 Diagnostic Error Message Description (MMU) (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		SR1 is checked to be zero, after executing an instruction that does not cause auto -incr/-decr of a register. SR2 is checked to be non-zero, since it tracks realtime virtual PC. A test for address conflict between SR0 and PSW is made and bus errors are reported. Test then checks for traps and bus errors caused by the above testing.	4	An MMU register contained unexpected (invalid) data.	
			6	An unexpected trap occurred while performing a stimulus.	
Test all MMU PARs and PDRs		Forces all PARs and PDRs to nonzero values and checks for a bus error, which indicates a negative response by register(s). The test performs a bit pattern test upon each register and checks for any effect upon other registers. A bit pattern failure is reported as a data error, and effect upon other registers as a bus error. A final check is made for bus errors and invalid trap errors (caused by testing process).	0	Either a MMU register failed to respond on the bus or a bus error was detected at the end of a stimulus.	
			4	An MMU register contained unexpected (invalid) data.	
			6	An unexpected trap occurred while performing a stimulus.	

Table 23-2. LSI 11/23 Diagnostic Error Message Description (MMU) (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
MAP	Test Kernel and User Mapping	First, performs a loop in which each address in the range 0-28KW is read via user space and compared with the same via kernel space (with comparison failures reported as 'map' errors). Second, performs a loop which writes each address value at that address (28-32KW), reads the value back and notes compare errors, 'bus' errors and invalid 'trap' errors.	2	Either a MMU register failed to respond on the bus or a bus error was detected at the end of a stimulus.	
			6	An unexpected trap occurred while performing a stimulus.	
			10	Values did not match when comparing data from user space and kernel space, or invalid address value detected during unique addressing test.	

SECTION XXIV
LRU TEST PROCEDURES
RLV12 CONTROLLER

24.1 GENERAL. This section contains test procedures for the RLV12 controller printed wiring board, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

24.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the RLV12:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01
Standard Quad Extender Board	DEC P/N W984-00
Disk, Scratch	DEC RL01

Tools other than standard shop tools are not required for test of the RLV12.

24.3 OTHER DOCUMENTATION. Refer to RLV12 Instruction Book (TI 6490.7) for detailed information and jumper configuration.

24.4 PREPARATION FOR TEST. To prepare the RLV12 for test, follow the instructions listed below.

1. Inspect the RLV12 Disk Controller for visual defects and correct jumper selections.
2. Verify that System Power switch is in ON position.
3. Set Electronics Chassis Power switch to OFF.
4. Disconnect MADTS system cable P/N 401-37778-01 from system RLV12 in slot A2-1 of Electronics Chassis card cage.
5. Remove system RLV12 from slot A2-1.
6. Insert quad extender board into slot A2-1, observe correct key polarity.
7. Insert RLV12 (unit under test) into extender board. Observe the correct key polarity so that CCA is oriented correctly with respect to its key.
8. Insert MADTS system cable P/N 401-37778-01 into RLV12 (unit under test).
9. Set Electronics Chassis Power switch to ON position.

24.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

```

SELFTEST [ CPU RAM REF PAT ADR INT CPY XFR ]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123
KD             *
KT             *
KP             *
MP             *.....
MR             .....*...
MS             **.....
RL             *???....

                0.....1.....2.....3.....4.....5.....6...
                012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

```

NOTE

Immediately after printout of the second unit number rule, PRESS the ESC key on the system LA34/LA100 in order to prevent the transitional boot of the disk-based MADTS. The allowed time period is approximately 2 seconds.

The MADTS is now ready to begin testing.

1. Input: D RL (CR)

Printer Response:

RL :

2. Input: P CNTL (CR)

Printer Response:

RLCNTL:

3. Input: X (CR)

Printer Response:

X.

00[--- >>> Drive under test is an RL01<<< ---
 . CSR BAR DAR MPR UNQ LPB INT OPI DCS WTA]

4. Remove the numbered, cammed ID button from the Unit Select Switch on the front panel of the RL01/RL02 Disk Drive.

Input: (CR)

Printer Response:

STA WTB

INSERT ID, Write ENABLE, Cover OPEN, then Press RETURN.

5. Insert the numbered, cammed ID button into the Unit Select Switch on the front panel of the RL01/RL02 Disk Drive. Verify that the 'fault' lamp is extinguished.
6. Set WRITE/PROTECT switch button to the OUT position on the front panel of the RL01/RL02 Disk Drive and verify that the button lamp is extinguished.
7. Set LOAD switch button to the OUT position on the front panel of the RL01/RL02 Disk Drive and verify that the button lamp is illuminated.
8. Open top assess-cover on disk drive. Leave open.

9. Input: (CR)

Printer Response:

STB WTC
Mount SCRATCH, Mode ONLINE, Write PROT, then
Press RETURN

10. Remove MADTS system RL01/RL02 Disk.
11. Mount a scratch RL01/RL02 Disk and close the assess cover.
12. Set LOAD button to the IN position and verify that the button lamp is extinguished.
13. Set the WRITE/PROTECT button to the IN position and verify that the button lamp is illuminated. Await the illumination of the 'ready' lamp and verify the 'fault' lamp is extinguished.
14. Input: .(CR)

Printer Response:

STC RDH HNF DAS WPE WTD
Write ENABLE, then Press RETURN

15. Set WRITE/PROTECT button to the OUT position and verify that the button lamp is extinguished with the 'fault' lamp illuminated.
16. Input: (CR)

Printer Response:

STD BAC WDS WCS RDS WDM WCM RDM DCK]

RLCNTL:

17. Verify that the 'fault' lamp is extinguished. The RLV12 Disk Controller diagnostic test is complete. If no error was reported by MADTS, the RLV12 is good.
18. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to Table 24-1, RLV12 Error Message. This table lists the test function, stimulus, and other information that may be contained in error message generated by the diagnostic program. Refer to the RLV12 Technical Description in the RLV12 Instruction Book (TI 6490.7) Volume II. Use accepted practices in isolation of faulty component(s).

24.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set LOAD button to OUT position on front panel of RL01/RL02 Disk Drive and wait for LOAD light to illuminate.
2. Set momentary BOOT/HALT switch on Electronics Chassis to HALT position.
3. Set Electronics Chassis Power switch to OFF position.
4. Disconnect MADTS system cable 401-37778-01 from RLV12 in slot A2-1 of Electronics Chassis.
5. Remove RLV12 (unit under test) from slot A2-1.
6. If additional RLV12 boards are to be tested, return to paragraph 24.4, step 7 and proceed. If not, continue Power Down Sequence.
7. Remove quad extender board from slot A2-1.
8. Insert MADTS system RLV12 into slot A2-1.
9. Insert MADTS system cable P/N 401-37778-01 into system RLV12.
10. Remove scratch RL01/RL02 Disk from drive.
11. Place MADTS system RL01/RL02 Disk into drive.
12. Set LOAD button to IN position.

24.7 MADTS DIGITAL RLV12 DISK CONTROLLER DIAGNOSTIC PROGRAM.

TYPE : DISC CONT
PART NUMBER : RLV12

I.D. : DISC CONTROLLER
CONFIGURE PER SPEC : 406-02154

24.7.1 Calling Sequence.

Device: RL
Program: CNTL

24.7.2 Function Mnemonics. The test function mnemonics used by the Digital disk drive controller diagnostic program are described below in the order of their occurrence. These tests require operator intervention for full execution. For the controller diagnostic tests, the disk drive is assumed to be fully operational. Before executing any RL diagnostic, perform drive prestartup inspection checklist and drive startup operations checklist described in the RLV12 Instruction Book (TI 6490.7).

<u>Mnemonic</u>	<u>Function Definitions</u>
a. CSR	Addressability & Bit Pattern Test of CSR Register
b. BAR	Addressability & Bit Pattern Test of BAR Register
c. DAR	Addressability & Bit Pattern Test of DAR Register
d. MPR	Addressability & Bit Pattern Test of MPR Register
e. UNQ	Unique Addressing of all Registers
f. LPB	Loop Back Selftest
g. INT	Interrupt Protocol
h. OPI	Operation-Incomplete Watchdog Timer
i. DCS	Generate Drive Command & Receive Status
j. WTA	Await -A: Drive w/o ID Plug
k. STA	Status-A: Drive w/o ID Plug
l. WTB	Await -B: Drive w/ ID Plug, Cover Open & Write Enable
m. STB	Status-B: Drive w/ ID Plug, Cover Open & Write Enable
n. WTC	Await -C: Drive Online w/SCRATCH & Write PROTECT
o. STC	Status-C: Drive Online w/SCRATCH & Write PROTECT
p. RDH	Read Header
q. HNF	Header Not Found Condition
r. DAS	Disk Address Send
s. WPE	Write Protect Error Condition
t. WTD	Await -D: Drive Online w/SCRATCH & Write Enable
u. BAC	Bus Address Counters
v. STD	Status-D: Drive Online w/SCRATCH & Write Enable
w. WDS	Write Data Single-Sector
x. WCS	Write Check Single-Sector
y. RDS	Read Data Single-Sector
z. WDM	Write Data Multiple-Sector
aa. WCM	Write Check Multiple-Sector
bb. RDM	Read Data Multiple-Sector
cc. DCK	Data Check Condition

24.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation is applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected. The stimulus for each function and its associated error data is given in Table 24-1. The address and contents of registers are normally given in the MADTS bit field dump format.

24.7.4 Error Output.

Error codes and any associated data are output as follows:

```
ERROR   #xx   DATA...DATA
```

Error codes are given in Table 24-1.

Table 24-1. RLV12 Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CSR	Register Test	Sets and resets each read/write bit in register using 'DATO', 'DATI' and 'DATIO' bus cycles.	0	Controller - access bus timeout error (controller is not available on the bus).	
			54	Register read/write bit test.	
BAR	Register Test	Sets and resets each read/write bit in register using 'DATO', 'DATI' and 'DATIO' bus cycles.	0	Controller - access bus timeout error (controller is not available on the bus).	
			54	Register read/write bit test.	
DAR	Register Test	Sets and resets each read/write bit in register using 'DATO', 'DATI' and 'DATIO' bus cycles.	0	Controller - access bus timeout error (controller is not available on the bus).	
			54	Register read/write bit test.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
MPR	Register Test	Access register using 'DATO', 'DATI' and 'DATIO' bus cycles.	0	Controller - access bus timeout error (controller is not available on the bus).	
UNQ	Register Test	Establish known data in each register. Modify each register while verifying that only the intended register is affected.	56	Non-unique register address.	
LPB	Digital Loopback	The 'Maintenance Function' is invoked as described in the RLV12 technical manual. All aspects of the function are verified as having been performed correctly. Function is invoked <u>without</u> 'Interrupt-Enable'.	4	Controller did not return to 'Ready' status within 1 second after function initiation.	
			12	Controller status reported an error.	
			16	Bus address register value was incorrect after operation.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			20	Disk address register value was incorrect after operation.	
			50	First section of test data pattern was erroneously modified.	'Actual' and 'Expected' patterns
			52	Last section of test data pattern was incorrect.	'Actual' and 'Expected' patterns
			58	Unexpected interrupt.	
			60	First reading of 'MPR' register indicates possible datapath error.	
			62	Second reading of 'MPR' register indicates possible FIFO serial output stage error.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
INT	Generate Interrupt	The 'Maintenance Function' (as described for 'LPB') is invoked with 'Interrupt-Enable'.	4	Interrupt did <u>not</u> occur within proper time interval.	
		MADTS verifies that a correct interrupt is generated within proper time interval and final controller status not in error.	6	Incorrect interrupt vector address.	
			12	Controller status error.	
OPI	Force 'OPI Watchdog Timer' Timeout Error	The 'Maintenance Function' is invoked with word-count chosen so as to result in 'OPI' status. 'Interrupt-Enable' is set. The OPI timer should time out in about 550 milliseconds after the operation has been initiated. If an interrupt timeout occurs, a timer failure is indicated. The accuracy of the timer is tested to verify +/-25% accuracy. If OPI did not occur, error 12 is issued.	4	Interrupt time out (1 second time allowance).	
			12	Controller status did <u>not</u> indicate 'OPI' error.	
			64	Time period out of bounds.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DCS	Get Status	Controller 'Get Status' Function is involved.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector addresss.	
WTA		Places message on the monitor and awaits the operator's response.			
STA	Get Status	Without the ID plug, the drive logically does not exist. The controller should return an error indication upon 'Get Status' function.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			12	Controller did <u>not</u> indicate an appropriate error.	
WTB		Places message on the monitor and awaits the operator's response.			
STB	Get Status	Status ID plug and cover open. With the cover open and ID plug reinserted, the status of the drive is checked.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			14	An error was reported to the controller by the drive.	0, Actual Drive Status, Expected Drive Status

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTC		Places message on the monitor and awaits the operator's response.			
STC	Get Status	Write Protect and Online status must be reported by the controller. The software will test for them and declare an error if they are absent.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			14	An error was reported to the controller by the drive.	0, Actual Drive Status, Expected Drive Status

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
RDH	Read Header	Header is read from current cylinder. If the header is read correctly, then no error will be reported.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			14	An error was reported to the controller by the drive.	0, Actual Drive Status, Expected Drive Status
HNF	Write Data	An illegal sector number is assigned and an attempt is made to write to that sector. The controller should time out and make a report of the header not found. If it does not, an error will be reported.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			8	Drive status <u>not</u> as expected.	
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual Drive Status, Expected Drive Status
DAS	Seek	A field of 1's with a 0 in it is rotated 15 times to present a pseudo-random disk address (Phase #1). Upon completion of this sequence, a field of 0's with a 1 in it is similarly rotated (Phase #2). At each cycle the response is tested by reading header to ensure that the head was sent to the proper address on the disk.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			10	Disk address found was not the one specified.	Phase #, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	Phase #, Actual Drive Status, Expected Drive Status, Actual Disk Address, Expected Disk Address
WPE	Write Data	A drive error should result if an attempt is made to write to a write-protected drive. The controller should detect and report the drive error; if it does not, then an error will be reported.	0	Bus error upon controller register access.	0, Actual Drive Status, Expected Drive Status
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	Drive error not reported.	
WTD		Places message on the monitor and awaits the operator's response.			
STD	Seek	The head is issued a seek to track 0. The status report will reflect the online and write enabled mode set by the operator in response to the message in the previous function.	0	Bus error upon controller register access.	
	Get Status		2	Controller not 'Ready'.	
			4	Interrupt timeout.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
BAC	Write Data	A shifting bit in the bus address register is used to set an address; a word read from each of 18 bus addresses is thus written on the disk. The bus address extensions are used, so that the CSR extension bits are tested.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	

Table 24-1. RLVL2 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WDS	Write Data	A pattern of data is generated and placed in memory. The 'Write Data' function is used to transfer the data pattern to the disk as single-sector operations throughout a full track.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			50	Pattern in memory was erroneously modified	
WCS	Write Check	The 'Write Check' function is applied to the data written previously as single-sector operations.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			50	Pattern in memory was erroneously modified.	
RDS	Read Data	The 'Read Data' function is applied to the data written previously as single-sector operations.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			52	Pattern read was in error.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WDM	Write Data	A pattern of data is generated and placed in memory. The 'Write Data' function is used to transfer the data pattern to the disk as multiple-sector operations throughout a full track.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			50	Pattern in memory was erroneously modified.	
WCM	Write Check	The 'Write Check' function is applied to the data previously written as multiple-sector operations.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			50	Pattern in memory was erroneously modified.	
RDM	Read Data	The 'Read Data' function is applied to the data previously written as multiple-sector operations.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	
			52	Pattern read was in error.	

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
DCK	Data Check	A pattern is set up in memory, written to the disk, then the data in memory is damaged by complementing the first word. The 'Write Check' function is invoked to compare the data from the disk to that in memory. If the incorrect data is not detected, a controller error is declared. Errors caused as composite or CRC errors are screened to eliminate confusion.	0	Bus error upon controller register access.	
			2	Controller not 'Ready'.	
			4	Interrupt timeout.	
			6	Incorrect interrupt vector address.	
			8	Drive status <u>not</u> as expected.	0, Actual Drive Status, Expected Drive Status
			10	Disk address found was not the one specified.	0, Actual and Expected Drive Status, Actual and Expected Disk Address
			12	Control status reported was not the one expected.	
			14	An error was reported to the controller by the drive.	0, Actual and Expected Drive Status, Actual and Expected Disk Address

Table 24-1. RLV12 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			16	Resultant 'BAR' incorrect.	
			18	Resultant 'BAE' incorrect.	
			20	Resultant 'DAR' incorrect.	

SECTION XXV
LRU TEST PROCEDURES
RL01/RL02 DISK DRIVE

25.1 GENERAL. This section contains test procedures for the RL01/RL02 Disk Drive, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

25.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the RL01/RL02 Disk Drive:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570
Disk Cartridge	DEC P/N RL01
Test Cable	DEC P/N BC80M-06
Cable Terminator	DEC P/N 70-12293

Tools other than standard shop tools are not required for test of the RL01/RL02 Disk Drive.

25.3 OTHER DOCUMENTATION. Refer to RL01/RL02 Disk Drive Instruction Book (TI 6490.7 Rev. A) for detailed information.

25.4 PREPARATION FOR TEST. To prepare the RL01/RL02 Disk Drive for test, follow the instructions listed below.

1. Perform procedure 2.8.3 steps 1 thru 6 (Page 2-37) in Drive Prestartup Inspection as described in User Guide in TI 6490.7 Rev. A.
2. Verify that MADTS System Power switch is in ON position.
3. Set Electronics Chassis Power switch to ON.

25.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

MADTS::U00.00 0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

KT *
KP *
MP *.....
MR*...
MS **.....
RL *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123

[COMMAND MODE]

NOTE

Immediately upon printout of the second unit number rule, press the ESC Key on the system LA34/LA100 in order to prevent the transitional boot of the disk-based MADTS. The allowed time period is approximately 2 seconds.

The MADTS is now ready to begin testing.

1. Input: D RL (CR)

Printer response:

RL :

2. Input: P DRIV (CR)

Printer response:

RLDRIV:

3. Ensure that the Power Switch on the RL01/RL02 Disk Drive (unit under test) is set to OFF.
4. Connect power cord of the RL01/RL02 Disk Drive (unit under test) to the utility outlet on the front of the MADTS.
5. Remove MADTS System cable, P/N 401-37778-01, P1 from the RLV12 board in slot A2-1 of the Electronics Chassis Card Cage.
6. Insert the correct end of the MADTS test cable, P/N BC80M-06 into the RLV12 board.
7. Insert the disk drive connector on MADTS Test Cable BC80M-06 into the top connector on the back of the RL01/RL02 Disk Drive (unit under test).
8. Insert cable terminator P/N 70-12293 into the bottom connector on the back of the RL01/RL02 Disk (unit under test).
9. Set Power Switch on the RL01/RL02 Disk Drive (unit under test) to ON.
10. Input: X (CR)

Printer response:

X.

00[

---->>>Device under test is an RL01<<<---
WTA

Inspection, Mount Scratch, Write PROT, ID,
Mode OFFLINE, then Press RETURN

NOTE

The diagnostic program will always output a message indicating whether the drive under test is an RL01 or RL02. It is the operator's responsibility to insure that the drive determination is correct.

11. Set LOAD button on the RL01/RL02 (unit under test) to the OUT position and verify that the button lamp is illuminated.
12. Press the WRITE/PROT button to the IN position and verify that the button lamp is illuminated.
13. Open Access Cover on RL01/RL02 (unit under test) and insert scratch disk after LOAD light illuminates. Close access cover. Verify that the FAULT lamp is extinguished.
14. Input: (CR)

Printer response:

STA WTB
Mode ONLINE, then Press RETURN

15. Press LOAD button to the IN position (unit under test) and wait for READY light to illuminate. Verify that the LOAD button lamp is extinguished and the Access Cover is locked.
16. Input: (CR)

Printer response:

STB GRD FLY WTC
Mode OFFLINE, Inspection, Mount STANDARDS, Mode ONLINE, then Press RETURN

17. Set LOAD button to the out position on the RL01/RL02 (unit under test) and wait for LOAD light to illuminate. Verify that the READY lamp is extinguished.
18. Open Access Cover on RL01/RL02 (unit under test) and remove scratch disk. Inspect drive READ/WRITE HEADS for dirt or damage. If any, take corrective action. Inspect surfaces of scratch disk for damage, if any, discard disk.
19. Insert a known good, formatted RL01/RL02 Disk (STANDARDS) or use the MADTS system RL01/RL02 disk and close access cover.
20. Set LOAD button to the IN position and wait for the READY light to illuminate. Verify that the LOAD button lamp is extinguished.
21. Ensure that the WRITE/PROT button is in the IN position.

22. Input: (CR)

Printer response:

STC SCR TRK CYL FLW WTD
Mode OFFLINE, Mount SCRATCH, Write enable, Mode
ONLINE, then Press RETURN

NOTE

This test requires approximately
five minutes for completion.

23. Set LOAD button to the OUT position and wait for the LOAD light to illuminate.
24. Remove Standards RL01/RL02 Disk.
25. Install scratch RL01/RL02 Disk.
26. Set WRITE/PROT button to the OUT position and verify that the lamp is extinguished.
27. Press LOAD button to the IN position and verify that the 'LOAD' lamp is extinguished. Wait for the illumination of the 'READY' lamp.
28. Input: (CR)

Printer response:

STD WRT IFR]

RLDRIV:

NOTE

This test requires approximately
five minutes for completion. RL02
testing will last somewhat longer,
due to the increased disk capacity.

29. The RL01/RL02 Disk Drive diagnostic test is complete. If no errors were reported by MADTS, the disk drive is good.
30. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to paragraph 25.7 and Table 25-1, RL01/RL02 Error Messages. This table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the Instruction Book TI 6490.7 Rev. A for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

25.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set LOAD button to OUT Position and wait for lamp to illuminate. Remove scratch RL01/RL02 disk from drive. Set Power Switch on rear of drive to OFF.
2. Set momentary BOOT/HALT switch to HALT position.
3. Set Electronics Chassis Power switch to OFF position.
4. Remove MADTS test Cable, BC80M-06 from RL01/RL02 Disk Drive (unit under test) and remove cable terminator.
5. If additional RL01/RL02 Disk Drives are to be tested, return to paragraph 25.5 step 7 and proceed.
6. Remove MADTS Test Cable BC80M-06 from RLV12 board in slot A2-1 in Electronics Chassis card cage.
7. Remove RL01/RL02 Disk Drive (unit under test) power cord from utility outlet on front of MADTS.
8. Insert MADTS system cable 401-37778-01, P1 onto RLV12 board.

25.7 MADTS DIGITAL RL01/RL02 DISK DIAGNOSTIC PROGRAM.

25.7.1 Calling Sequence.

Device: RL
Program: DRIV

25.7.2 Function Mnemonics. The test function mnemonics used by the DIGITAL disk drive diagnostic program are described below in the order of their occurrence. These tests require operator intervention and mounting a scratch disk as necessary. The RLV12 controller is assumed to be fully operational.

PROGRAM FUNCTIONS

<u>Mnemonic</u>	<u>Function</u>
a. WTA	Await DRIVE OFFLINE with scratch pack
b. STA	Test nominal OFFLINE DRIVE status
c. WTB	Await DRIVE ONLINE with scratch pack
d. STB	Test nominal ONLINE DRIVE status
e. GRD	Test Guard-band detection and response

f.	FLY	Test head-flying capability
g.	WTC	Await DRIVE ONLINE with standards pack
h.	STC	Test nominal ONLINE DRIVE status
i.	SCR	Test ability to search for and read sectors
j.	TRK	Test ability to select tracks and read sectors
k.	CYL	Test ability to seek cylinders and read sectors
l.	FLW	Test ability to follow cylinder ("LWEAR TRACKING")
m.	WTD	Await DRIVE ONLINE w/scratch pack
n.	STD	Test nominal ONLINE drive status
o.	WRT	Test ability to write sectors
p.	IFR	Test adjacent-cylinder READ/WRITE interference
q.	FMT	Test and initialize diskpack

25.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation which may result in an error condition. Detection of an error after excitation has been applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected by the MADTS specialist. The stimulus for each function and its associated error data are as follows. The address and contents of registers are normally given in the MADTS BIT FIELD DUMP FORMAT. This allows detailed analysis of the error condition reported by the diagnostic. The stimuli for each function and associated error data is given in Table 25-1.

25.7.4 Error Output. Error codes and any associated data are output in the form:

Error #xx DATA...DATA

Error codes used by the MADTS RL01/RL02 Disk Drive diagnostic program and their associated output parameters are given in Table 25-1.

Table 25-1. RL01/RL02 Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTA		Requests the operator to place the system in OFF-LINE mode and mount a scratch disk. No tests are conducted; the system awaits operator action and proceeds to the next function when the action has been completed.			
STA	Get status	The status of the drive is tested.	8	Drive status error	0, Actual drive status, Expected drive status
			12	Control status reported was not the one expected. Consider the possibility that the drive may not be responsive to controller signals.	
			14	An error was reported to the controller by the drive.	0, Actual drive status, Expected drive status
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTB		Requests the operator to change mode to "online," then resumes operation when the interaction has been completed.			
STB	Get status	The status of the drive is tested.	8	Drive status	0, Actual drive status, Expected drive status
			14	An error was reported to the controlled by the drive.	0, Actual drive status, Expected drive status
			22	Drive not ready	
GRD	Seek	A seek is initiated to the outer guard band from the current position of the head. A second seek is made; then the same sequence is followed to the inner guard band. Following this, another pair of seeks to the outer guard band is made, ensuring that two full sweep seeks are made to test the detection and handling of the guard bands.	8	Drive status	0, Actual drive status, Expected drive status
			14	Drive error	0, Actual drive status, Expected drive status
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
FLY	Seek	Various patterns are used to vigorously exercise the head seek operation, and ability of heads to "fly".	8	Drive status	0, Actual drive status, Expected drive status
			14	Drive error	0, Actual drive status, Expected drive status
			22	Drive not ready	
WTC		Requests the operator to place the disk in online mode after mounting a standards disk. When the operator has complied, operation will resume.			
STC	Get Status	The status of the drive is tested.	8	Drive status	0, Actual drive status, Expected drive status
			14	Drive error	0, Actual drive status, Expected drive status
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
SCR	Read	Test ability of read circuitry.	8	Drive status	1, Actual drive status, Expected drive status
			10	Disk address found was not the one specified.	2, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	2, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	
TRK	Read and Select Heads	Test ability to select heads (change tracks)	8	Drive status	1, Actual drive status, Expected drive status
			10	Disk address found was not the one specified.	2, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	2, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CYL	Seek and Read	Test ability to seek cylinders.	8	Drive status	Phase #, Actual drive status, Expected drive status
			10	Disk address found was not the one specified.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	
FLW	Seek and Read	Test ability to 'Track Follow' at various disk addresses.	8	Drive status	Phase #, Actual drive status, Expected drive status
			10	Disk address found was not the one specified.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
WTD		The operator is requested to mount a scratch disk with WRITE enabled in ON-LINE mode. Upon receipt of RETURN the test operation continues.			
STD	Get Status	The status of the drive is tested.	8	Drive status	0, Actual drive status, Expected drive status
			14	An error was reported to the controller by the drive.	0, Actual drive status, Expected drive status
			22	Drive not ready	
WRT	Seek, Select Head, Write and Read	Test ability to write and read-back data at various disk addresses. A test for 'read-reduction' is also performed by reading the data repeatedly.	8	Drive status	Phase #, Actual drive status, Expected drive status
			10	Disk address found was was not the one specified.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	

Table 25-1. RL01/RL02 Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
IFR	Seek, Select Head, Write and Read	An 'adjacent cylinder interference' test is performed.	8	Drive status	Phase #, Actual drive status, Expected drive status
			10	Disk address found was not the one specified.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			14	An error was reported to the controller by the drive.	Phase #, Actual drive status, Expected drive status, Actual disk address, Expected disk address
			22	Drive not ready	

SECTION XXVI
LRU TEST PROCEDURES
MULTIPLEXER INTERFACE

26.1 GENERAL. This section contains test procedures for the Multiplexer Interface, P/N 401-37170. This interface consists of two circuit card assemblies, P/N 401-36968. Each one is MADTS testable.

The following test procedure can be used in two ways. The first way is to test a CCA which has been removed from the Multiplexer Interface assembly. The second way is to test both of the CCAs, one at a time, while installed in the assembly. The following test procedure is written assuming the CCA has been removed from the assembly. However, by referring to Table 26-2 the corresponding connector numbers may be found for the -01 or the -02 Multiplexer I/F assembly. By substituting the corresponding assembly connector number for the connector number called out in paragraphs 26.4 and 26.5, each CCA may be tested while remaining in the assembly.

The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

26.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Multiplexer Interface:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
Patch Panel Cable	DEC P/N DPC-32-3
MADTS	E-Systems P/N 401-37570-01
Ribbon Test Cable	E-Systems P/N 401-37142-02
Test Cable	E-Systems P/N 401-37881-01
Power Test Cable	E-Systems P/N 401-37739-01
Multimeter	Fluke 8021B (or equivalent)

26.3 OTHER DOCUMENTATION. Refer to M1FC FSAS Equipment Instruction Book, TI 6490.37 for detailed information on the Multiplexer Interface.

26.4 PREPARATION FOR TEST. To prepare the Multiplexer Interface CCA for test, follow the instructions listed below:

1. Verify that system Power switch is set to ON position.
2. Set Electronics Chassis Power switch to OFF.

3. Set Modem E-208A (in Card Cage RM-8E, slot 1) switches to following positions:
 - a. ST/STRO switch to NORM
 - b. AL/DL switch to NORM
4. Connect Digital Patch Panel cable DPC-32-3 from Digital Patch Panel position RM-8E SLOT 1 to Digital Patch Panel MUX INTERFACE patch cable jack.
5. Lift MADTS system Multiplexer CCA about half way out of slot A2-2 in MADTS card cage, making connector numbers on Multiplexer visible.
6. Disconnect ribbon cable P/N 401-37759-01, 1A2W9, P-2 from J-2 on MADTS system Multiplexer CCA and ribbon cable P/N 401-37759-01, 1A2W10, P-2 from J-1 on MADTS system Multiplexer CCA.
7. Connect ribbon test cable P/N 401-37142-02 P-1 to J-2 on MADTS system Multiplexer CCA. Connect second ribbon test cable P/N 401-37142-02 P-1 to J-1 on MADTS system Multiplexer CCA.
8. Insert MADTS system multiplexer CCA into slot A2-2 in Electronics Chassis card cage.
9. Connect test cable P/N 401-37881-01 P-2 to Digital Patch Panel 37-pin "D" connector MUX INTERFACE.
10. Connect Power test cable P/N 401-37739-01 P-2, P-3, and P-4 to GND, +5V, and -12V, respectively, on I/O Control Panel.
11. Connect power test cable P/N 401-37739-01 P-1 (coming from I/O Control Panel) to J-7 on Multiplexer Interface CCA under test.
12. Connect test cable P/N 401-37881-01 P-1 (coming from Digital Patch Panel) to J-6 on Multiplexer Interface CCA under test. Digital Patch Panel position MUX INTERFACE and J-6 on Multiplexer Interface CCA are now connected.
13. Connect ribbon test cable P/N 401-37142-02 P-2 (coming from J-2 on MADTS system Multiplexer CCA) to J-3 on Multiplexer Interface CCA under test. J-2 on MADTS system Multiplexer CCA and J-3 on the Multiplexer Interface CCA are now connected. Connect second ribbon test cable P/N 401-37142-02 P-2 (coming from J-1 on MADTS system

Multiplexer CCA) to J-4 on Multiplexer Interface CCA under test. J-1 on MADTS system Multiplexer CCA and J-4 on Multiplexer CCA are now connected.

14. Set Electronics Chassis Power switch to ON.

26.5 TEST PROCEDURES. When the Power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

?

e

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              -
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              -
TK              -

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MX (CR)

Printer response:

MXDIAG:

2. Input: S EU=3 (CR)

Printer response:

S EU=3.

3. Input: X (CR)

Printer response:

X.
00[CSR
CP Unit Number is 02

INT HDL TRN TRE ADR DLY
Press Return to Continue

NOTE

The ADR function is applicable to M1FC
MUX boards only. If a Model 1 board
is under test, ADR should be disabled
(S-ADR).

4. Disconnect test cable P/N 401-37881-01 P1 from J-6 on the Multiplexer Interface CCA under test.
5. Reconnect P-1 on the test cable to J-5 on the Multiplexer Interface CCA under test. Digital Patch Panel position MUX INTERFACE and J-5 on the Multiplexer Interface CCA are now connected.
6. Cycle ST/STRO switch on Modem E-208A in Card Cage RM-8E, slot 1. (Set ST/STRO switch to STRO, then to ST, and then back to NORM).

7. Input: (CR)

Printer response:

.
]
01[CSR
CP Unit Number is 02

Printer response (continued):

INT HDL TRN TRE ADR DLY
Press Return to Continue

8. Disconnect test cable P/N 401-37881-01 P-1 from J-2 on the Multiplexer Interface CCA under test.
9. Reconnect P-1 on the test cable to J-2 on the Multiplexer Interface CCA under test. Digital Patch Panel position MUX INTERFACE and J-2 on the Multiplexer Interface CCA are now connected.
10. Cycle ST/STRO switch on Modem E-208A in Card Cage RM-8E, slot 1.
11. Input: (CR)

Printer response:

.
]
02[CSR
CP Unit Number is 02

INT HDL TRN TRE ADR DLY
Press Return to Continue

12. Disconnect test cable P/N 401-37881-01, P-1 from J-2 on the Multiplexer Interface CCA under test.
13. Reconnect P-1 on the test cable to J-1 on the Multiplexer Interface CCA under test. The Digital Patch Panel position MUX INTERFACE and J-1 on the Multiplexer Interface CCA are now connected.
14. Cycle ST/STRO switch on Modem E-208A, in Card Cage RM-8E, slot 1.
15. Input: (CR)

Printer response:

.
]
03[CSR
CP Unit Number is 02

INT HDL TRN TRE ADR DLY
Press RETURN to Continue

16. Input: (CR)

Printer response:

```

      .
      ]
MXDIAG:

```

17. On the Multiplexer Interface CCA (unit under test), measure the voltage from either end of R3 to ground with a Digital Multimeter, and verify that the voltage is $+5.0 \pm 1.0$ VDC.
18. On the Multiplexer Interface CCA (unit under test), measure the voltage from either end of R1 to ground with a Digital Multimeter, and verify that the voltage is -5.0 ± 1.0 VDC.
19. Upon successful completion of this test procedure the Multiplexer Interface CCA (unit under test) is good.
20. If an error is detected by the diagnostic, an error message is generated. To interpret the error message, refer to Section 10, paragraph 10.1, and Table 10-2 for the MUX Diagnostic Error Messages. The table lists the test function, stimulus, and other information that may be contained in error messages generated by the diagnostic program. Refer to the M1FC FSAS Equipment Instruction Book (TI 6490.37) for theory of operation to assist in troubleshooting. Use accepted practices in isolation of faulty component(s).

26.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Set momentary BOOT/HALT switch to HALT position.
2. Set Electronics Chassis Power switch to OFF position.
3. Disconnect ribbon test cable P/N 401-37142-02 P-2 from J-3 on Multiplexer Interface CCA under test, and disconnect ribbon test cable P/N 401-37142-02 P-2 from J-4 on Multiplexer Interface CCA under test.
4. Disconnect test cable P/N 401-37881-01 P-1 from J-1 on Multiplexer Interface CCA under test.
5. Disconnect Power test cable P/N 401-37739-01 P-1 from J-7 on Multiplexer Interface CCA under test.

6. If additional Multiplexer Interface CCAs are to be tested return to paragraph 26.4, step 11 and repeat test with next Multiplexer Interface CCA. Otherwise continue Power Down Sequence.
7. Remove Digital Patch Panel cable P/N DPC-32-Y from Digital Patch Panel.
8. Remove test cable P/N 401-37881-01 P-2 from Digital Patch Panel 37-pin "D" connector MUX INTERFACE.
9. Remove Power test cable P/N 401-37739-01 from I/O Control Panel.
10. Lift MADTS system Multiplexer CCA about half way out of slot A2-2 in MADTS card cage, making connector numbers on Multiplexer visible.
11. Remove both ribbon test cables, P/N 401-37142-02 from J-1 and J-2 on MADTS system Multiplexer CCA.
12. Connect ribbon cable P/N 401-37759-01, 1A2W9, P-2 to J-2 on MADTS system Multiplexer CCA, and connect ribbon cable P/N 401-37759-01, 1A2W10, P-2 to J-1 on MADTS system Multiplexer CCA.
13. Insert MADTS system Multiplexer CCA into slot A2-2 in Electronics Chassis card cage.

Table 26-1. MUX Diagnostic Error Message Description

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
CSR	Read CSR	The MUX Control Status Register is read.	0	A bus timeout occurred while trying to read the MUX is not usable.	-
	Write to CSR	An Octal 60 is written to the CSR.	2	A bus timeout occurred while attempting to write the CSR.	CSR contents (BFD)
INT	Initialize MUX	The MUX is reset. A time interval of 2/60 of a second is allowed for the CSR Done bit to be set. The vector base address and the control/status segment base address is sent to the MUX via the CSR. Again, a 2/60 of a second time interval is allowed for the CSR Done bit to be set. All interrupts are then enabled.	4	The Done bit in the CSR was not set within 2/60 of a second. The MUX is not usable.	CSR contents (BFD)

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
LPB	Enable Loop-back	MUX on-board loopback is enabled. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loop-back status is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			10	An incorrect loop-back status was returned by the MUX after being put in the loopback mode.	Channel number under test
HDL	Enable HDLC Mode	The mode byte in the Channel Control Segment is set to indicate HDLC. The transmit service required byte is set and the CSR is strobed. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The channel mode is checked via the channel status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test The interrupt vector received
			12	An incorrect channel mode value was returned by the MUX.	Channel number under test Expected channel mode value (3) Channel mode value returned by the MUX

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
TRN	Transmit	A transmit operation is initiated with the transmit data and the receive buffer in non-extended memory. A time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector is then verified. A channel receive request is then made. A time interval of 5 seconds is also allowed for a receive interrupt to be generated by the MUX. The interrupt vector is then verified. The channel status segment is accessed to check for a transmit or receive error. The data received is then compared with the data transmitted.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test vector address received
			20	A transmit error occurred.	First three words of the channel status segment
			14	An expected receive interrupt was not received within the allotted time.	Channel number under test
			16	The receive interrupt was the wrong interrupt.	Channel number under test Interrupt vector received.

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
			22	A receive error occurred.	Channel number under test 5th thru 7th words of channel status segment
			18	Data received does not match the data transmitted.	64 words of transmit buffer 64 words of receive buffer Channel number under test
TRE	Transmit	A transmit operation is initiated with the transmit data and the receive buffer in extended memory a time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector then is verified. A channel request is made, and a time interval of 5 seconds is allowed for a receive interrupt to be generated by the MUX. The channel status segment is accessed to check	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			20	A transmit error occurred.	Channel number under test First three words of channel status segment

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
		for a transmit or receive error. The data received is then compared with the data transmitted.			
			14	An expected receive interrupt was not received within the allotted time.	Channel number under test
			16	The receive interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received.
			22	A receive error occurred.	Channel number under test 5th thru 7th words of channel status segment
			18	Data received does not match the data transmitted.	64 words of transmit buffer 64 words of receive buffer Channel number under test

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
ADR	ADR1	MUX address search is enabled. An invalid header address is transmitted. No receive interrupt should occur and no message should be received.	24	Message not filtered while in address search mode.	Channel No. Message header address
	ADR2	MUX address search is enabled. A valid header address is transmitted. The data is received and verified.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			20	A transmit error occurred.	Channel number under test First three words of channel status segment
			26	Data transfer error while in address search mode.	64 words of transmit buffer 64 words of receive buffer Channel number under test

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
RLB	Disable Loop-back	MUX on-board loopback is disabled. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loopback is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			10	An incorrect loopback status was returned by the MUX after loopback mode being remove.	Channel number under test
PRI	Enable printer mode	The selected channel is put into printer mode. A time interval of 5 seconds is allowed for an interrupt to be generated by the MUX. The interrupt vector is then verified. The loopback status is verified via the MUX status segment.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test Interrupt vector received
			12	An incorrect channel mode value was returned by the MUX.	Channel number under test The expected channel mode value (1) the channel mode value returned by the MUX

Table 26-1. MUX Diagnostic Error Message Description (Continued)

Test Function	Stimulus	Operation	Error Msg #	Error	Error Msg Additional Data
TPR	Test printer mode	A transmit operation is initiated with the transmit data and the channel already in the printer mode. A time interval of 5 seconds is allowed for a transmit interrupt to be generated by the MUX. The interrupt vector then is verified. The channel Status Segment is accessed to check for a transmit error.	6	An expected transmit interrupt was not received within the allotted time.	Channel number under test
			8	The transmit interrupt received was the wrong interrupt.	Channel number under test vector address received
			20	A transmit error occurred.	Channel number under test First three words of the channel status segment
DLY	Delay execution	A message is output to the console directing the operator to type a character when execution is to be continued. Execution of the diagnostic with resume when a character is entered.	none		

Table 26-2. Test Connector Substituting Table

Multiplexer I/F CCA 401-3698-01 Test Connections	Multiplexer I/F Assembly 401-37170-01 Test Connectors		Multiplexer I/F Assembly 401-37170-04 Test Connectors	
	Left Side	Right Side	Left Side	Right Side
J1	J7	J11	J11	J7
J2	J8	J12	J12	J8
J3	J15	J17	J17	J15
J4	J16	J18	J18	J16
J5	J9	J13	J13	J9
J6	J10	J14	J14	J10
J7	J5	J6	J6	J5

SECTION XXVII
LRU TEST PROCEDURES
DEC RL01/RL02 DISK CARTRIDGE

27.1 GENERAL. This section contains test procedures for the DEC RL01/RL02 Disk Cartridge, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which has several functions that will be very useful in troubleshooting as well as testing. These functions will be explained in subsequent paragraphs.

27.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the DEC RL01/RL02 Disk Cartridge:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01

Tools other than standard shop tools are not required for test of the RL01/RL02 Disk Cartridge.

27.3 OTHER DOCUMENTATION. Refer to RL01/RL02 Disk Drive Instruction Book, TI 6490.7 for detailed information on the RL01/RL02 Disk Cartridge.

27.4 PREPARATION FOR TEST. To prepare the disk cartridge for test, follow the instructions below:

1. Verify that System Power switch is set to ON position.
2. Set Electronic Chassis Power switch to ON position.

27.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]
Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

NOTE

Immediately upon printout of the second unit number rule, press the ESC key on the system LA34/LA100 in order to prevent the transitional boot of the disk-Based MADTS. The allowed time period is approximately 2 seconds.

The MADTS is now ready to begin testing.

1. Input: D RL (CR)

Printer response:

RL :

2. Input: P DRIV (CR)

Printer response:

RLDRIV:

3. Input: S -*+FMT (CR)

Printer response

RLDRIV:

4. Set LOAD button to out position and wait for LOAD light to come on.

5. Remove MADTS System DEC RL01/RL02 Disk Cartridge.

6. Install DEC RL01/RL02 Disk Cartridge (unit under test). Inspect both disk surfaces for damage or contamination and take any necessary corrective action.

7. Set LOAD button to the in position, and wait for READY light to come on. Listen for any unusual sounds during spinup and take corrective action as needed. Ensure drive is not write-protected.

NOTE

This test requires approximately twenty minutes for completion. There will be 8 columns of numbers under the BAD SECTOR FILE heading.

8. Input: X (CR)

Printer response:

```
X.
00[
--- >>>Drive under test is an RL01<<< ---
FMT*
Index      BAD SECTOR FILE
000000     *****
000020     *****
000040     *****
000060     *****
000100     *****
```

```

000120  *****  *****  *****  ...
000140  *****  *****  *****  ...
000160  *****  *****  *****  ...
000200  *****  *****  *****  ...
000220  *****  *****  *****  ...
000240  *****  *****  *****  ...
000260  *****  *****  *****  ...
000300  *****  *****  *****  ...
000320  *****  *****  *****  ...
000340  *****  *****  *****  ...
000360  *****  *****  *****  ...
]

```

RLDRIV:

NOTE

The diagnostic program will always output a message indicating whether the drive under test is an RL01 or RL02. It is the operator's responsibility to insure that the drive determination is correct.

9. Upon successful completion of this test procedure, the DEC RL01/RL02 Disk Cartridge (unit under test) is good.
10. If a bad disk cartridge is detected during the test, replace cartridge. A bad disk is indicated by any of the following errors: 10, 14, 24, 26, 28. Drive and controller are assumed to be operating properly. Note that the "Bad Sector File" printout alone does not indicate a bad cartridge. The latter is indicated only by an "Error" message.

27.6 POWER DOWN SEQUENCE. Upon TEST COMPLETION, follow these steps:

1. Set LOAD button to out position, and wait for LOAD light to come on.
2. Remove DEC RL01/RL02 Disk Cartridge (unit under test). Inspect drive heads and disk surfaces for dirt or damage and take corrective action if necessary.
3. If additional DEC RL01/RL02 Disk Cartridges are to be tested, return to paragraph 27.5, step 6, and repeat test with next DEC RL01 Disk Cartridge. Otherwise, continue Power Down Sequence.
4. Set momentary BOOT/HALT switch to HALT position.

5. Install MADTS System DEC RL01/RL02 Disk Cartridge.
6. Set LOAD button to IN position.
7. Set Electronics Chassis Power switch to OFF position.

27.7 MADTS DEC RL01/RL02 DISK CARTRIDGE DIAGNOSTIC PROGRAM.

27.7.1 Calling Sequence.

Device: RL
Program: DRIV

27.7.2 Function Mnemonics. The test-function mnemonics used by the Digital Disk Drive is also used to perform diagnostics on the RL01/RL02 Disk Cartridge. These tests require operator intervention for full execution; a confidence check is conducted and reported prior to the MADTS prompt displayed on the monitor. Before executing any RL diagnostic, perform drive prestartup inspection checklist and drive startup operations checklist. Refer to Section 25, Disk Drive Diagnostics, paragraph 25.7 and Table 25-1 for error definitions and procedures.

27.7.3 Function Stimuli Descriptions. A function tests a single portion of a device's operation. Each function consists of one or more stimuli. A stimulus is defined as an operation that can result in an error condition. Detection of an error after excitation is applied causes error information to be output to the console. The diagnostic then suspends, aborts the test, loops on the function, or loops on the stimulus, depending on the options selected by the MADTS specialist. The address and contents of registers are normally given in the MADTS bit field dump format. This allows detailed analysis of the error condition reported by the diagnostic by referring to Section 25, paragraph 25.7 and Table 25-1.

The error codes are assigned by evaluation routines which test the validity of the data collected as an indication of operations performed by the test item.

27.7.4 Error Output. Error codes and any associated data are output as follows:

ERROR #xx DATA...DATA

The error codes used by the MADTS RL01/RL02 Disk Cartridge diagnostic program and their associated output parameters are given in Section 25, paragraph 25.7 and Table 25-1.

SECTION XXVIII
LRU TEST PROCEDURES
UDS RM-9600 MODEM

28.1 GENERAL. This section contains test procedures for the UDS RM-9600 Modem, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which will simulate operation of the modem under normal conditions.

28.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the UDS RM-9600 Modem:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01

Tools other than standard shop tools are not required for test of the UDS RM-9600 Modem.

28.3 OTHER DOCUMENTATION. Refer to RM-8E Multiple Modem System Instruction Book (TI 6490.38) for detailed information on the RM-9600 Modem.

28.4 PREPARATION FOR TEST. To prepare the UDS RM-9600 Modem for test, follow the instructions listed below:

1. Verify that RM-9600 Modem Card, P/N 2092284 (unit under test) is configured as in Figure 28-1.
2. Verify that system Power switch is set to ON position.
3. Remove MADTS system RM-208A Modem from slot 1 of RM-8E Modem Enclosure.
4. Set Electronics Chassis Power switch to ON position.

28.5 TEST PROCEDURES. When the Power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

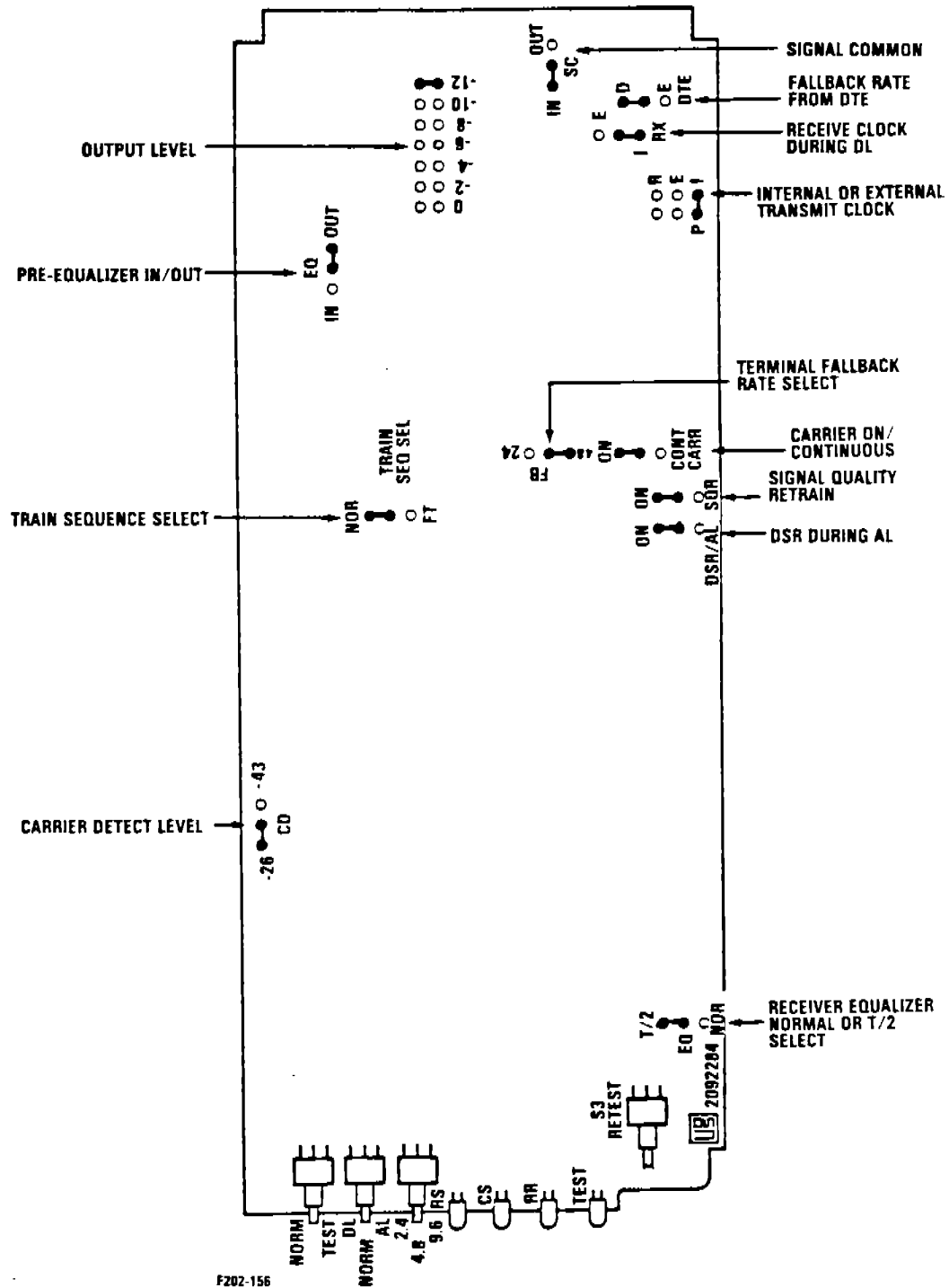


Figure 28-1. RM-9600 Card P/N 2092284 Jumper Configuration

3.

B

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]

Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```

MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???.

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123

```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

```

.SET TT QUIET
DFX SYSTEM LOAD UTILITY
<133134>=SPACE

```

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```

MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???.
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123

```

[COMMAND MODE]

:

1. Input: D MX (CR)

Printer response:

MXDIAG:

2. Input: S -EU (CR)

Printer response:

MXDIAG:

3. Insert RM-9600 Modem (unit under test) into slot 1 of the RM-8E Modem Enclosure.
4. Set front panel modem switches (unit under test) as follows:
 - a. NORM/TEST switch to NORM
 - b. DL/AL switch to NORM
 - c. 2.4/4.8/9.6 switch to 9.6

5. Input: X (CR)

Printer response:

X.
00[CSR
CP Unit Number is 03

INT HDL TRN TRE ADR DLY
Press Return to Continue

6. Input: (CR)

Printer response:

]
MXDIAG:

NOTE

The ADR function is applicable to M1FC MUX boards only. If a Model 1 board is under test, ADR should be disabled (S-ADR).

7. Upon successful completion of this test procedure the RM-9600 Modem under test is good.

8. If an error is indicated by the RM-9600 Modem LED indicators, refer to Section IV of the RM-8E Multiple Modem System Instruction Book, TI 6490.38. Use accepted practices in isolation of faulty component(s).

28.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Remove RM-9600 Modem (unit under test) from slot 1 of RM-8E Modem Enclosure.
2. If additional boards are to be tested, return to paragraph 28.4 and repeat test. Otherwise, continue with Power Down Sequence.
3. Insert MADTS system RM-208A Modem into slot 1 of RM-8E Modem Enclosure.
4. Set momentary BOOT/HALT switch to HALT position.
5. Set Electronics Chassis Power switch to OFF position.

SECTION XXIX
LRU TEST PROCEDURES
UDS E-208A MODEM
AND E-A/O CARD

29.1 GENERAL. This section contains test procedures for the E-208A Modem and the E-A/O card as tested on the MADTS. The test is conducted under software control, which will simulate operation of the modem under normal conditions.

29.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the E-208A and E-A/O Modems:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01

Four Phone Lines

"A" Refers to the phone number connected to the TELCO connector 6 on back of RM-8E Modem Enclosure.

"B" Refers to the phone number connected to the TELCO connector 6A on back of RM-8E Modem Enclosure.

Tools other than standard shop tools are not required for test of the E-208A and E-A/O Modems.

29.3 OTHER DOCUMENTATION. Refer to RM-8E Multiple Modem System Instruction Book (TI 6490.38) for detailed information on the E-208A and E-A/O Modems.

29.4 PREPARATION FOR TEST.

1. Verify that E-208A Modem Card, P/N 2082278 (unit under test) is configured as in Figure 29-1.
2. Verify that E-A/O Modem Card, P/N 1020364 (unit under test) is configured as in Figure 29-2 or that it is configured as in Figure 29-3.
3. Verify that System Power switch is set to ON position.
4. Verify that RM-8E Power Supply is ON.
5. Connect the 25-pin "D" connector on end of cord coming from MADTS System phone to Manual Call Unit connector on Digital Patch Panel, and screw down connector to panel.
6. Set Electronics Chassis Power switch to ON position.

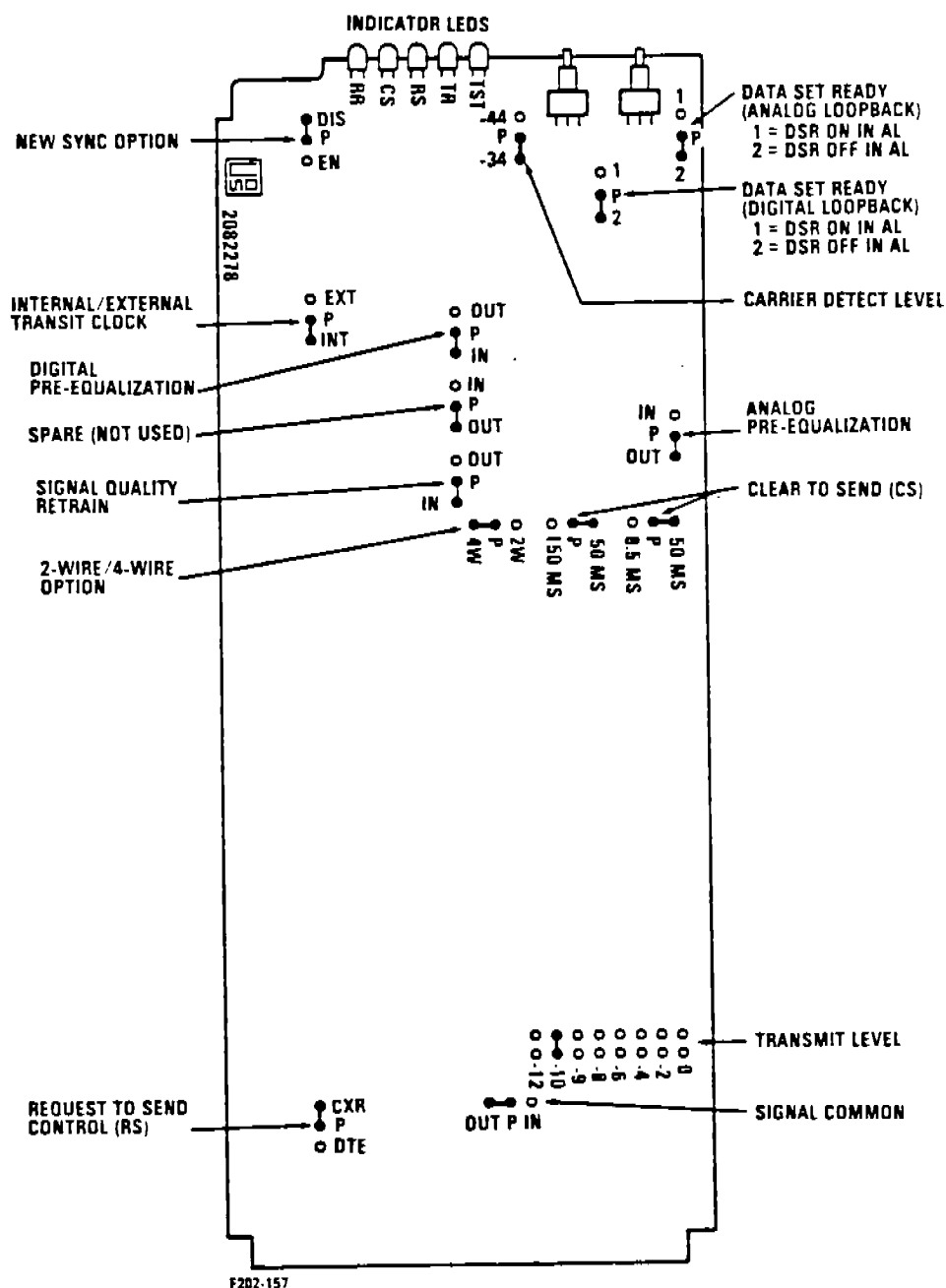


Figure 29-1. E-208A Card P/N 2082278 Jumper Configuration

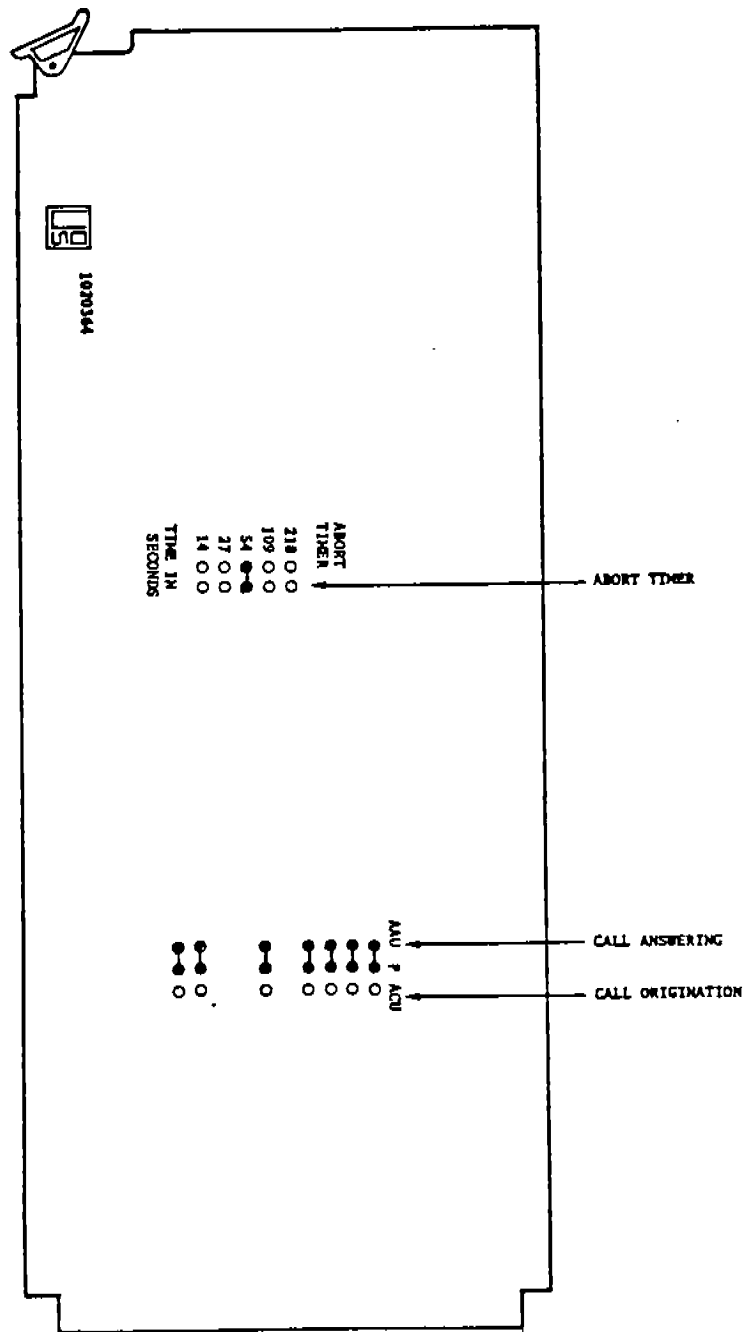


Figure 29-2. E-A/O Card P/N 1020364 Jumper Configuration - AFSS

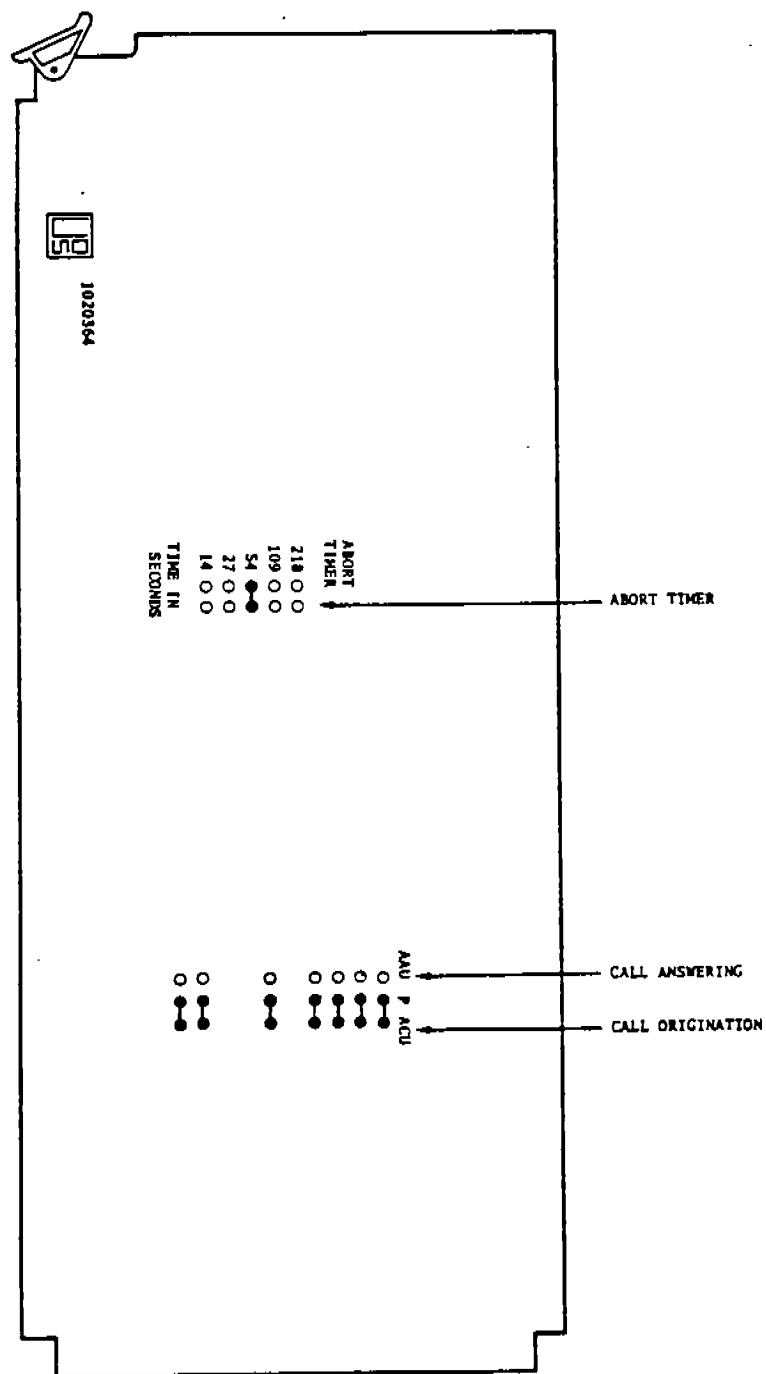


Figure 29-3. E-A/O Card P/N 1020364 Jumper Configuration - FSDPS

29.5 TEST PROCEDURES. When the power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

2.

2

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]

Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

0.....1.....2.....3.....4.....5.....6...
0123456789012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET

DFX SYSTEM LOAD UTILITY

<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

0.....1.....2.....3.....4.....5.....6...
0123456789012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MX (CR)

Printer response:

MXDIAG:

2. Insert E-208A Modem (unit under test) into slot 3 of the RM-8E Modem enclosure.
3. Set the front panel E-208A Modem switches (unit under test) as follows:
 - a. NORM/TEST switch to NORM
 - b. DL/AL switch to NORM

4. Input: S -EU+SU=1 (CR)

Printer response:

MXDIAG:

5. Input: X (CR)

Printer response:

X.
01[CSR
CP Unit Number is 02

INT HDL TRN TRE ADR DLY
Press return to continue

6. Input: (CR)

Printer response:

]

MXDIAG:

NOTE

The ADR function applies to M1FC MUX boards only. It should be disabled when testing with a Model 1 MUX.

7. If the E-A/O Modem Card under test is jumpered for the FSDPS configuration (auto call unit), proceed to paragraph 29.5.2. If the E-A/O is jumpered for the AFSS configuration (auto answer unit), proceed to paragraph 29.5.1.

29.5.1 AFSS (Auto Answer Unit) Configuration

1. Verify EMCU switch is in BUS position.
2. Remove the E-208A Modem (unit under test) from slot 3 and insert it into slot 5 of the RM-8E Modem Enclosure.
3. Insert E-A/O card (unit under test) into slot 6 of the RM-8E Modem Enclosure.
4. Move the MADTS system E-208A Modem from slot 1 to slot 7 of the RM-8E Modem Enclosure.
5. Verify that the MADTS system E-A/O card in slot 2 of the RM-8E Modem Enclosure is jumpered for the FSDPS configuration.
6. Insert the MADTS system E-A/O card into slot 8.
7. Input: S -*SU-EU (CR)
Printer response:
MXDIAG:
8. Input: S +CSR+INT+HDL (CR)
Printer response:
MXDIAG:
9. Input: X (CR)
Printer response:
X.
00[CSR
CP Unit Number is 02
INT HDL]
MXDIAG:
10. Input: S EU=3-CSR-INT (CR)
Printer response:
MXDIAG:

11. Input: X (CR)

Printer response:

X.
00[HDL]
01[HDL]
02[HDL]
03[HDL]

MXDIAG:

12. Verify that the TR lights on the E-208A Modems in slots 5 and 7 are ON.

NOTE

The dial tone and modem tone referred to in the following steps have a 3 to 5 second duration. The action (dial number of press/raise exclusion key) must be within the time limit otherwise the operator will be required to return to step 6 and repeat test.

13. Lift phone receiver.
14. Dial 8.
15. Raise exclusion key (the white hookswitch on the phone).
16. Verify the phone has a dial tone.
17. Dial phone number "A" 2088 (refer to paragraph 29.2).
18. Wait for the number to answer and the modem tone.
19. Press exclusion key down during tone and release.
20. Dial 7.
21. Raise exclusion key.
22. Verify the phone has a dial tone.
23. Dial phone number "B" 2089 (refer to paragraph 29.2).
24. Wait for the number to answer and the modem tone.

25. Press the exclusion key down during modem tone and verify the RR light on the E-208A Modem in slot 7 blinks once.
26. Hang up receiver.
27. Upon successful completion of this test procedure the UDS E-208A Modem and E-A/O card (units under test) are good.

29.5.2 FSDPS (Auto Call Unit) Configuration.

1. Move the E-208A Modem (unit under test) from slot 3 to slot 7 of the RM-8E Modem Enclosure.
2. Insert E-A/O card (unit under test) into slot 8 of the RM-8E Modem Enclosure.
3. Move the MADTS system E-208A Modem from slot 1 to slot 5 of the RM-8E Modem Enclosure.
4. Verify that the MADTS system E-A/O card in slot 2 of the RM-8E Modem Enclosure is jumpered for the AFSS configuration.

5. Insert the MADTS system E-A/O card into slot 6.

6. Input: S -* -SU-EU (CR)

Printer response:

MXDIAG:

7. Input: S +CSR+INT+HDL (CR)

Printer response:

MXDIAG:

8. Input: X (CR)

Printer response:

X.
 00[CSR
 CP Unit Number is 02
 INT HDL]

MXDIAG:

9. Input: S EU=3-CSR-INT (CR)

Printer response:

MXDIAG:

10. Input: X (CR)

Printer response:

X.
00 [HDL]
01 [HDL]
02 [HDL]
03 [HDL]

MXDIAG:

11. Verify that the TR lights on the E-208A Modems in slots 5 and 7 are ON.

NOTE

The dial tone and modem tone referred to in the following steps have a 3 to 5 second duration. The action (dial number of press/raise exclusion key) must be within the time limit otherwise the operator will be required to return to step 6 and repeat test.

12. Lift phone receiver.
13. Dial 8.
14. Raise exclusion key (the white hookswitch on the phone).
15. Verify the phone has a dial tone.
16. Dial phone number "A" (refer to paragraph 29.2).
17. Wait for the number to answer and the modem tone.
18. Press exclusion key down during tone and release.
19. Dial 7.
20. Raise exclusion key.
21. Verify the phone has a dial tone.
22. Dial phone number "B" (refer to paragraph 29.2).
23. Wait for the number to answer and the modem tone.

24. Press the exclusion key down during dial tone and verify the RR light on the E-208A Modem in slot 7 blinks once.
25. Hang up receiver.
26. Upon successful completion of this test procedure the UDS E-208A Modem and E-A/O card (units under test) are good.

29.6 POWER DOWN SEQUENCE (AFSS CONFIGURATION).

Upon test completion follow these steps:

1. Remove E-208A (unit under test) from slot 5 of RM-8E Modem Enclosure.
2. Remove E-A/O (unit under test) from slot 6 of RM-8E Modem Enclosure.
3. Move MADTS system E-208A Modem from slot 7 to slot 1 of RM-8E Modem Enclosure.
4. Move MADTS system E-A/O card from slot 8 to slot 2 of RM-8E Modem Enclosure.
5. Input: (ESC)

Printer response:

\$

MX :

6. Input: (ESC)

Printer response:

\$

7. If additional E-208A and E-A/Os are to be tested, inspect next E-208A and E-A/O (see paragraph 29.4) and return to preparation for test, paragraph 29.4 and repeat test. Otherwise, continue Power Down Sequence.
8. Remove phone cord from Digital Patch Panel 25-pin "D" connector, Manual Call Unit.

29.7 POWER DOWN SEQUENCE (FSDPS CONFIGURATION).

Upon test completion follow these steps.

1. Remove E-208A (unit under test) from slot 7 of RM-8E Modem Enclosure.

2. Remove E-A/O (unit under test) from slot 8 of RM-8E Modem Enclosure.
3. Move MADTS system E-208A Modem from slot 5 to slot 1.
4. Move MADTS system E-A/O card from slot 6 to slot 2.
5. Input: (ESC)

Printer response:

\$

MX :

6. Input: (ESC)

Printer response:

\$

:

7. If additional E-208A and E-A/Os are to be tested, inspect next E-208A and E-A/O cards (see paragraph 29.4) and return to preparation for test, paragraph 29.4 and repeat test. Otherwise, continue Power Down Sequence.
8. Remove phone cord from Digital Patch Panel 25-pin "D" connector, Manual Call Unit.

SECTION XXX
LRU TEST PROCEDURES
UDS MANUAL CALL UNIT (MCU)

30.1 GENERAL. This section contains the test procedure for the UDS Manual Call Unit, P/N 1020377, as tested by the MADTS. The test is conducted under software control, which allows the MCU to function as if it were in the MIFC FSAS system.

30.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the MCU CCA:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostic Test Set (MADTS)	E-Systems P/N 401-37570-01

Four Phone Lines

"A" Refers to the phone number connected to the TELCO connector 6 on the back of the RM-8E Modem Enclosure.

Tools other than standard shop tools are not required for test.

30.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the RM-8E Multiple Modem System Instruction Book (TI 6490.38).

30.4 PREPARATION FOR TEST. To prepare the MCU CCA for test, follow the instructions listed below.

1. Verify that MADTS system E-A/O card in slot 2 of RM-8E Modem Enclosure is configured for FSDPS. See Figure 29-3.
2. Verify that system power switch is in ON position.
3. Verify that RM-8E Power Supply is ON.
4. Set Electronics Chassis Power Switch to ON position.

30.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following typical message:

2-

@

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]

Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET

DFX SYSTEM LOAD UTILITY

<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ****....
RL              *???....
TA              .
TK              .

                  0.....1.....2.....3.....4.....5.....6...
                  012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D MX (CR)

Printer response:

MXDIAG:

2. Connect the 25-pin "D" connector on the end of the cord coming from the MADTS system phone to the Manual Call Unit connector on the Digital Patch Panel, and screw down the connector to the panel.
3. Move the MADTS system E-208A modem from slot 1 to slot 7 in the RM-8E Modem Enclosure.
4. Set the front panel E-208A Modem switches (unit in slot 7) as follows:
 - a. NORM/TEST switch to NORM.
 - b. DL/AL switch to NORM.
5. Move the MADTS system E-A/O card from slot 2 to slot 8 in the RM-8E Modem Enclosure.
6. Remove the MADTS system MCU from slot 0 of the RM-8E Modem Enclosure.
7. Insert the MCU (unit under test) into slot 0 of the RM-8E Modem Enclosure.
8. Set the MCU BUS/LINE switch to BUS.
9. Input: S -*--SU-EU (CR)

Printer response:

MXDIAG:

10. Input: S +CSR+INT+HDL (CR)

Printer response:

MXDIAG:

11. Input: X (CR)

Printer response:

X.
00[CSR
CP Unit Number is 03

INT HDL]

MXDIAG:

12. Input: S EU=3-CSR-INT(CR)

Printer response:

MXDIAG:

13. Input: X (CR)

Printer response:

X.
00 [HDL]
01 [HDL]
02 [HDL]
03 [HDL]

MXDIAG:

14. Verify that the TR light on the E-208A modem in slot 7 of the RM-8E Modem Enclosure is ON.

NOTE

The dial tone and modem tone referred to in the following steps have a 3 to 5 second duration. The action (dial number or press/raise exclusion key) must be within the time limit otherwise the operator will be required to start at step 9 and repeat test.

15. Lift phone receiver.
16. Dial 8.
17. Raise exclusion key (white hook switch on the phone).
18. Verify the Talk Mode light on the MCU (unit under test) is ON.

19. Verify the phone has a dial tone.
20. Dial phone number "A" (see paragraph 30.2).
21. Verify the phone number rings.
22. Hang up receiver.
23. Upon successful completion of this test procedure the UDS Manual Call Unit (unit under test) is good.

30.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps.

1. Remove MCU (unit under test) from slot 0 of RM-8E Modem Enclosure.
2. If additional MCUs are to be tested return to paragraph 30.4 and repeat test. Otherwise, continue Power Down Sequence.
3. Replace MADTS system MCU into slot 0 of RM-8E Modem Enclosure.
4. Move MADTS system E-208A modem from slot 7 to slot 1 of RM-8E Modem Enclosure.
5. Move MADTS system E-A/O card from slot 8 to slot 2 of RM-8E Modem Enclosure.
6. Remove phone cord from Digital Patch Panel 25-pin "D" connector, MANUAL CALL UNIT.

SECTION XXXI
LRU TEST PROCEDURES
DISPLAY MONITOR

31.1 GENERAL. This section contains the test procedures for the Display Monitor P/N TTL-150, as tested by the MADTS. The test is conducted under software control, which has several functions that are very useful in troubleshooting as well as testing. These functions are explained in subsequent paragraphs.

31.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the Display Monitor:

<u>Test Equipment</u>	<u>Manufacturer and Part No.</u>
Maintenance and Diagnostic Test Set (MADTS)	E-Systems P/N 401-37570-01
Coax Cables	401-37797-02
Coax Cables	401-37797-02
Coax Cables	401-37797-02

Tools other than standard shop tools are not required for test.

31.3 OTHER DOCUMENTATION. Other documentation required for test or troubleshooting is the TTL-150 Display Monitor Instruction Book (TI 6490.15). 0056-00-471-4000

31.4 PREPARATION FOR TEST. To prepare the Display Monitor for test, follow the instructions listed below.

1. Verify that System Power switch is in ON position.
2. Set Electronics Chassis Power switch to OFF.
3. Connect three coax cables P/N 401-37797-02, from Display Monitor to I/O Control Panel for HORIZONTAL SYNC, VERTICAL SYNC and VIDEO, respectively.
4. Insert Display Monitor power cord into 110 VAC outlet, and turn the Display Monitor Power switch (in upper left corner) clockwise.
5. Set I/O Control Panel switches in accordance with Table 31-1.

31.5 TEST PROCEDURE. When the power switch on the Electronics Chassis is set to the ON position the MADTS will auto boot and prompt the operator with the following message:

Table 31-1. Initial Switch Settings

<u>SWITCH</u>	<u>POSITION</u>
1. KEYBOARD	X
2. SYNC SELECT	OTF PROCESSOR
3. SYSTEM ADDRESS BIM	X
4. SYSTEM ADDRESS CACHE	1-4
5. VIDEO SELECT	SYSTEM CACHE
6. ELECTRONICS CHASSIS POWER	ON

X = Any Position

?

0

SELFTEST [CPU RAM REF PAT ADR INT CPY XFR]

Maintenance and Diagnostic Test System / FSAS Model 1 [DEPOT PROM]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  01234567890123456789012345678901234567890123
KD              *
KT              *
KP              *
MP              *.....
MR              .....*...
MS              **.....
RL              *???....
```

```
0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

: D RL.

RL : B.

RT-11SJ (S) V04.00

.SET TT QUIET

DFX SYSTEM LOAD UTILITY

<133134>=SPACE

Maintenance and Diagnostic Test System / FSAS Model 1 [Depot Disk]

```
MADTS::V00.00  0.....1.....2.....3.....4.....5.....6...
                  01234567890123456789012345678901234567890123
KD              *
KT              *
AN              .....????****
CI              .
DL              .....*****
FP              *
IP              *..
KB              *
KP              *
LA              *
LP              *
MP              *.....
MR              .....*...
MS              **.....
MX              ***....
RL              *???....
TA              .
TK              .
```

```
0.....1.....2.....3.....4.....5.....6...
012345678901234567890123456789012345678901234567890123
```

[COMMAND MODE]

:

The MADTS is now ready to begin testing.

1. Input: D AN (CR)

Printer response:

AN :

2. Input: P DISP (CR)

Printer response:

ANDISP:

3. Input: S SU=41-EU-#+PAT (CR)

Printer response:

ANDISP:

4. Input: X (CR)

Printer response:

X.

41[PAT

Press Return to Continue

NOTE

Upon diagnostic initiation, detection of a Model 1 OTF/Cache will result in an appropriate message indication to the console.

5. After approximately 20 seconds of warmup time, adjust the intensity and contrast of the monitor to the desired level.
6. Verify that the Display Monitor is the same as Figure 31-1. Check the center and corners of the display for good focus and linearity. The display field should measure about 10 inches horizontally and 7.5 inches vertically. (This will almost fill the screen.)
7. Input: (CR)

Printer response:

]

ANDISP:

```

ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./01
BCDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./012
CDEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123
DEFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./01234
EFGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./012345
FGHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456
GHIJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./01234567
HJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./012345678
IJKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:
KLMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?
PQRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@
QRSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@A
RSTUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@AB
STUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABC
TUVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABCD
UVWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABCDE
VWXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABCDEF
WXYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFG
XYZ[\]^_`abcdefghijklmnopqrstuvwxyz-|-| !"#$%&'()*+,-./0123456789:;<=>?@ABCDEFGH

```

Figure 31-1. Pattern (PAT)

This line demonstrates the CURSOR attribute
 This line demonstrates the BACKGROUND attribute
 This line demonstrates the REVERSE VIDEO attribute
 This line demonstrates the BLINKING attribute
 This line demonstrates the EMPHASIS attribute

```

ABCDEFGHIJKLMNPOQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012
BCDEFGHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012
CDEFGHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123
DEFGHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./01234
EFGHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012345
FGHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456
GHIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./01234567
HIJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./012345678
IJKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789
JKLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:
KLMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;
LMNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<
MNOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=
NOPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>
OPQRSTUVWXYZ[\]~"abcdefghijklmnopqrstuvwxyz-!@!#$%^&'()*+,-./0123456789:;<=>?
  
```

Figure 31-2. Attribute Test Pattern (ATD)

- NOTE:
1. The word CURSOR should have a cursor (underscore) that blinks at the rate of 1.25 Hz (0.8 seconds cycle time). Text lines 1, 6, and 11 should also have the cursor attribute.
 2. The word BACKGROUND should be at half the normal intensity. Lines 2, 7, and 12 should also have the background attribute.
 3. The words REVERSE VIDEO should be black-on-green. Lines 3, 8 and 13 should also have the reverse video attribute.
 4. The word BLINKING should blink at the rate of 1.25 Hz (0.8 seconds cycle time). Lines 4, 9, and 14 should also have the blink attribute.
 5. The word EMPHASIS should be "flickering" (intensity modulating) at the rate of 3 Hz. Lines 5, 10, and 15 should also have the emphasis attribute.

SECTION XXXII
LRU TEST PROCEDURES
UDS RM-9600E FP MODEM

32.1 GENERAL. This section contains test procedures for the UDS RM-9600E FP Modem, as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which will simulate operation of the modem under normal conditions.

32.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the UDS RM-9600E FP Modem:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01

Tools other than standard shop tools are not required for test of the UDS RM-9600E FP Modem.

32.3 OTHER DOCUMENTATION. Refer to RM-8E Multiple Modem System Instruction Book, (TI 6490.38) for detailed information on the RM-9600E FP Modem.

32.4 PREPARATION FOR TEST. To prepare the the UDS RM-9600E FP Modem for test, follow the instructions below:

1. Verify that RM-9600E FP Modem Card, P/N 2092842 (unit under test) is configured as in Figure 32-1.
2. Verify that system power switch is set to ON position.
3. Remove MADTS system RM-208A Modem from slot 1 of RM-8E Modem Enclosure.
4. Set Electronics Chassis Power switch to ON position.

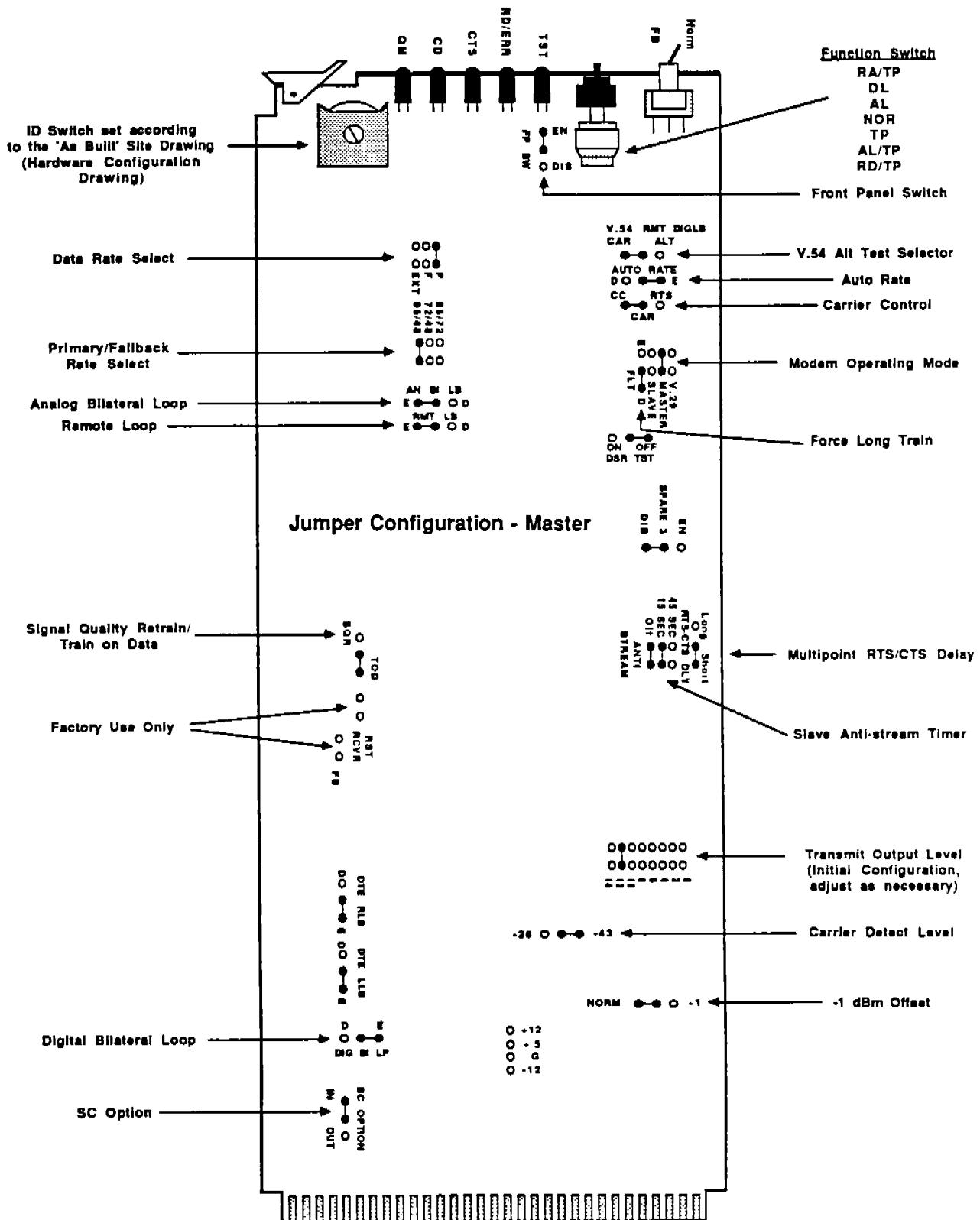


Figure 32-1. RM-9600E FP Modem Card P/N 2092842
Jumper Configuration (Sheet 1 of 2)

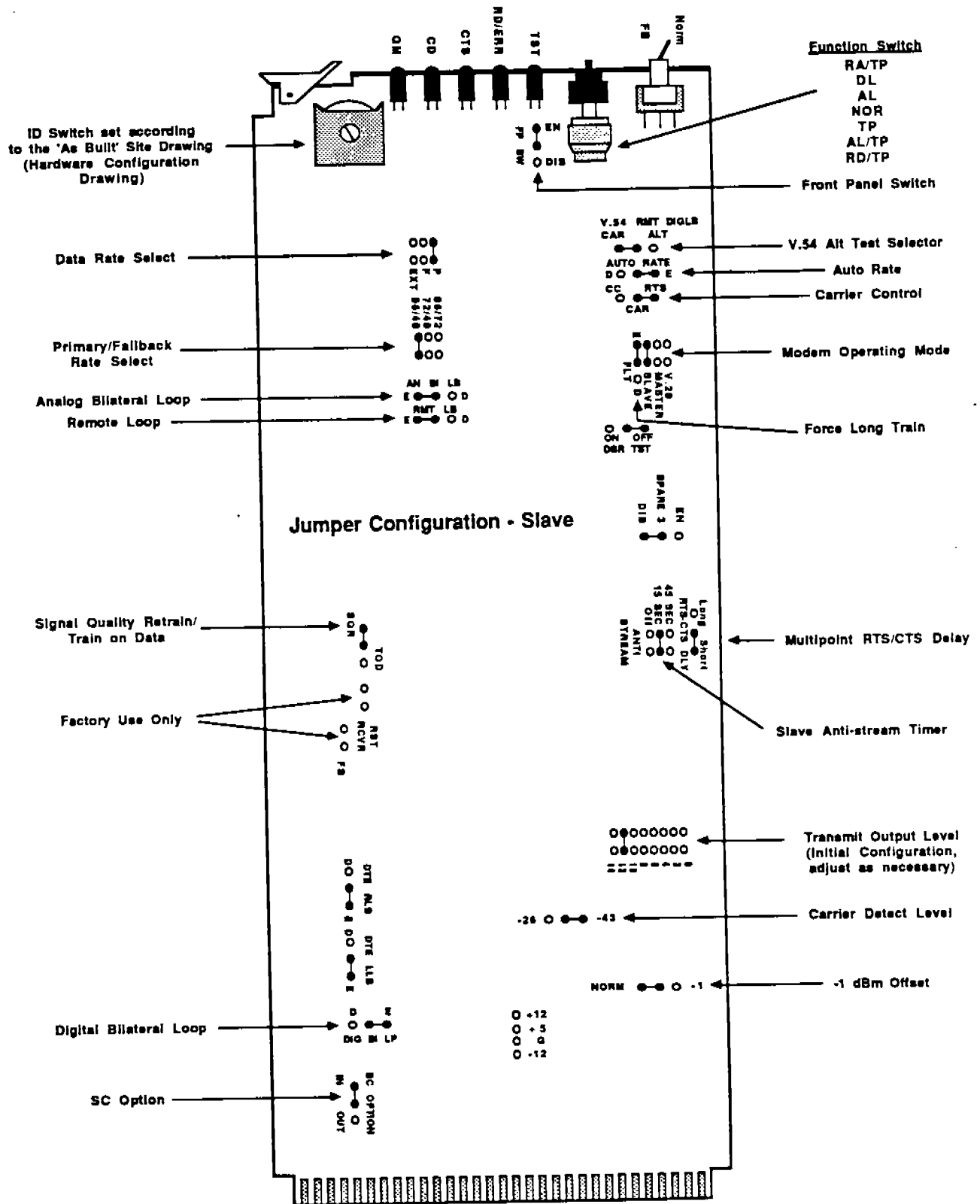


Figure 32-1. RM-9600E FP Modem Card P/N 2092842
Jumper Configuration (Sheet 2 of 2)

32.5 TEST PROCEDURES. When the Power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

1. Operator Input: D MX (CR)

Printer response:

P DIAG:

MXDIAG:

2. Operator Input: S SU=1-EU (CR)

Printer response:

S SU=1-EU

MXDIAG:

3. Insert RM-9600E FP Modem (unit under test) into slot 3 of the RM-8E Modem Enclosure.

4. Set the RM-9600E FP modem switches to the following positions:

- a. NORM/FB switch to NORM

- b. Rotary Function switch to NOR

5. Operator Input: X (CR)

Printer response:

X.
01[CSR
CP Unit Number is 03

INT HDL TRN TRE ADR DLY
Press RETURN to Continue

6. Operator Input: (CR)

Printer response:

]

MXDIAG:

NOTE

The ADR function is applicable to M1FC MUX boards only. If a Model 1 board is under test, ADR should be disabled (S-ADR).

7. Upon successful completion of this test procedure the RM-9600E FP Modem under test is good.
8. If an error is indicated by the RM-9600E FP Modem LED indicators, refer to Section IV of the RM-8E Multiple Modem System Instruction Book, TI 6490.38. Use accepted practices in isolation of faulty component(s).

32.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Remove RM-9600E FP Modem (unit under test) from slot 3 of RM-8E Modem Enclosure.
2. If additional boards are to be tested, return to paragraph 32.4 and repeat test. Otherwise, continue with Power Down Sequence.
3. Set momentary BOOT/HALT switch to HALT position.
4. Set Electronics Chassis Power switch to OFF position.

SECTION XXXIII
LRU TEST PROCEDURES
UDS MODEM SHARING DEVICE (MSD)

33.1 GENERAL. This section contains test procedures for the UDS Modem Sharing Device (MSD), as tested on the MADTS, P/N 401-37570. The test is conducted under software control, which will simulate operation of the modem under normal conditions.

33.2 TEST EQUIPMENT AND TOOLS REQUIRED. The following test equipment is required for test of the MSD:

<u>Test Equipment</u>	<u>Manufacturer and Model No.</u>
MADTS	E-Systems P/N 401-37570-01

Tools other than standard shop tools are not required for test of the MSD.

33.3 OTHER DOCUMENTATION. Refer to RM-8E Multiple Modem Sharing Device Instruction Book (TI 6490.40) for detailed information on the MSD.

33.4 PREPARATION FOR TEST. To prepare the the UDS MSD for test, follow the instructions below:

1. Verify that System POWER switch is set to ON position.
2. Verify that RM-8E Modem Enclosure POWER is ON.
3. Connect 32 circuit patch cord, P/N DPC-32-3, between RM-8E slot 1 jack and MUX INTERFACE jack on Digital Patch Panel.
4. Connect MUX Interface cable, P/N 401-37881-01, between MUX INTERFACE 37-pin connector on Digital Patch Panel and MODEM 37-pin connector on MSD.
5. Connect 32 Circuit Patch Cord, P/N DPC-32-M-6FT-M2 between MUX CHANNEL 0 jack on Digital Patch Panel and Port 1 37-pin connector on MSD.
6. Connect MSD AC power cord to utility power outlet below RL01/RL02 Disk Drive in MADTS (or any 120 VAC, 60 Hz power outlet).
7. Set Electronics Chassis Power switch to ON position.

33.5 TEST PROCEDURES. When the Power switch on the Electronics Chassis is set to the ON position, the MADTS will auto boot and prompt the operator with the following typical message:

1. Operator Input: D MX (CR)

Printer response:

P DIAG:

MXDIAG:

2. Set the front panel E-208A Modem switches as follows:

- a. NORM/TEST switch to NORM

- b. DL/AL switch to NOR

3. Operator Input: S SU=0-EU-ADR (CR)

Printer response:

S SU=0-EU-ADR

MXDIAG:

4. Operator Input: S -DLY+LP (CR)

Printer response:

S -DLY+LP

MXDIAG:

5. Operator Input: X (CR)

Printer response:

```

X.
00[ CSR
CP Unit Number is 03

INT HDL TRN TRE ]
00[ CSR
CP Unit Number is 03

INT HDL TRN TRE ]
00[ CSR
CP Unit Number is 03

INT HDL TRN TRE ]
00[ CSR
CP Unit Number is 03

INT HDL TRN TRE ]
00[ CSR
CP Unit Number is 03

INT HDL TRN TRE ]
00[ CSR
CP Unit Number is 03

```

Observe: E-208A Modem TR RS CS and RR LEDs and the Modem Sharing Device RTS LED flash during each test loop

6. Input: ESC (Halts Test)

Printer response:

:

7. Input: ESC (Returns to restart test)

Printer response:

MXDIAG:

8. Remove 32 circuit patch cord from Port 1 and install on Port 2 on the Modem Sharing Device.
9. Repeat steps 5 through 7.
10. Remove 32 circuit patch cord from Port 2 and install on Port 3 on the Modem Sharing Device.
11. Repeat steps 5 through 7.
12. Upon successful completion of this test procedure the Modem Sharing Device under test is good.

33.6 POWER DOWN SEQUENCE.

Upon TEST COMPLETION follow these steps:

1. Remove all cables from MSD.
2. Remove MSD power cord from AC outlet.
3. If additional MSDs are to be tested, return to paragraph 33.4 and repeat test. Otherwise, continue with Power Down Sequence.
4. Remove cables from MADTS Digital Patch Panel.
5. Set momentary BOOT/HALT switch to HALT position.
6. Set Electronic Chassis power switch to OFF position.